Advanced Lithographic Patterning and Resolution Limits

MICRO-724 (2025)
Advanced topics in micro- and nanomanufacturing: top-down meets bottom-up

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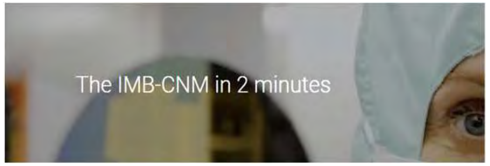

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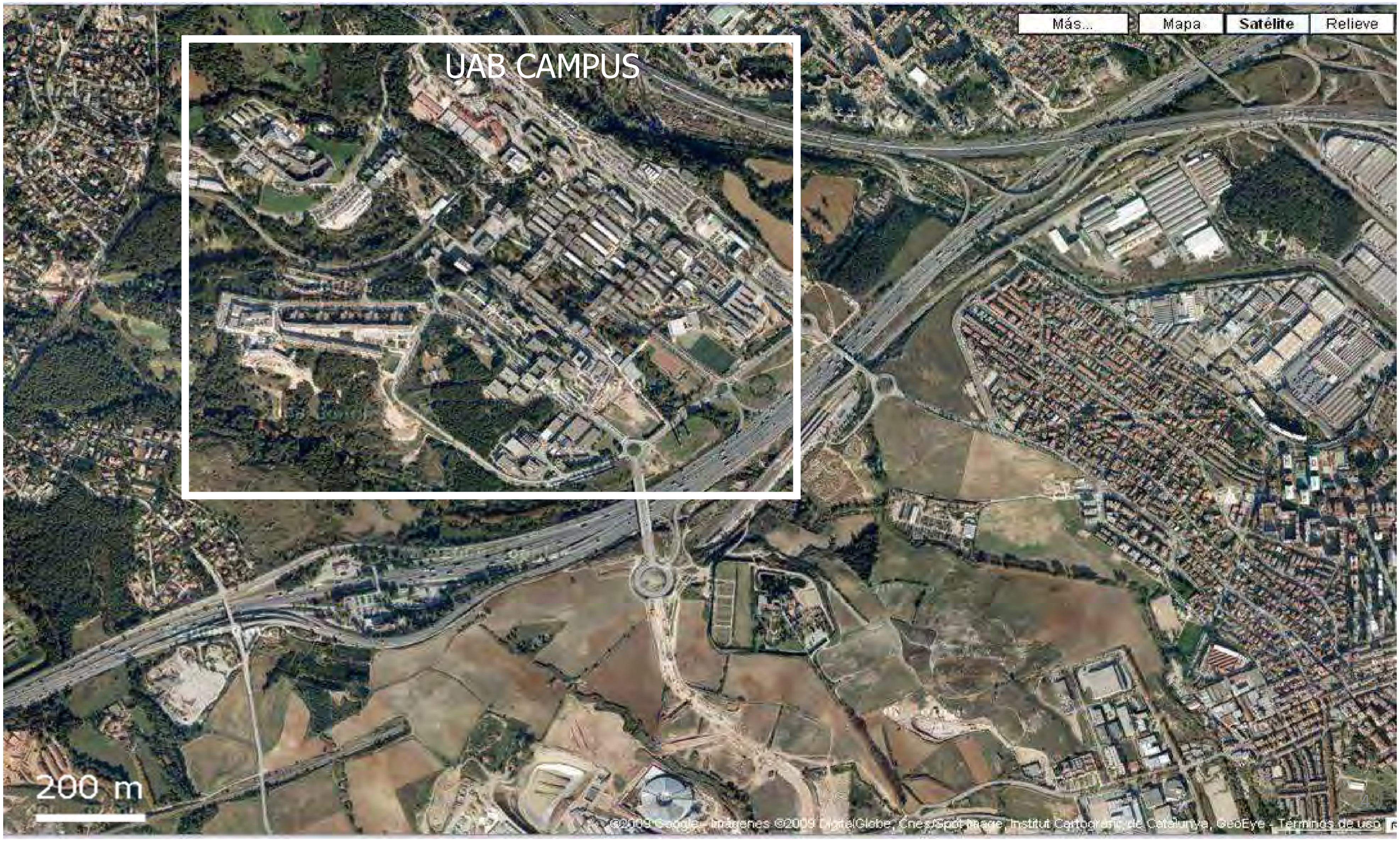
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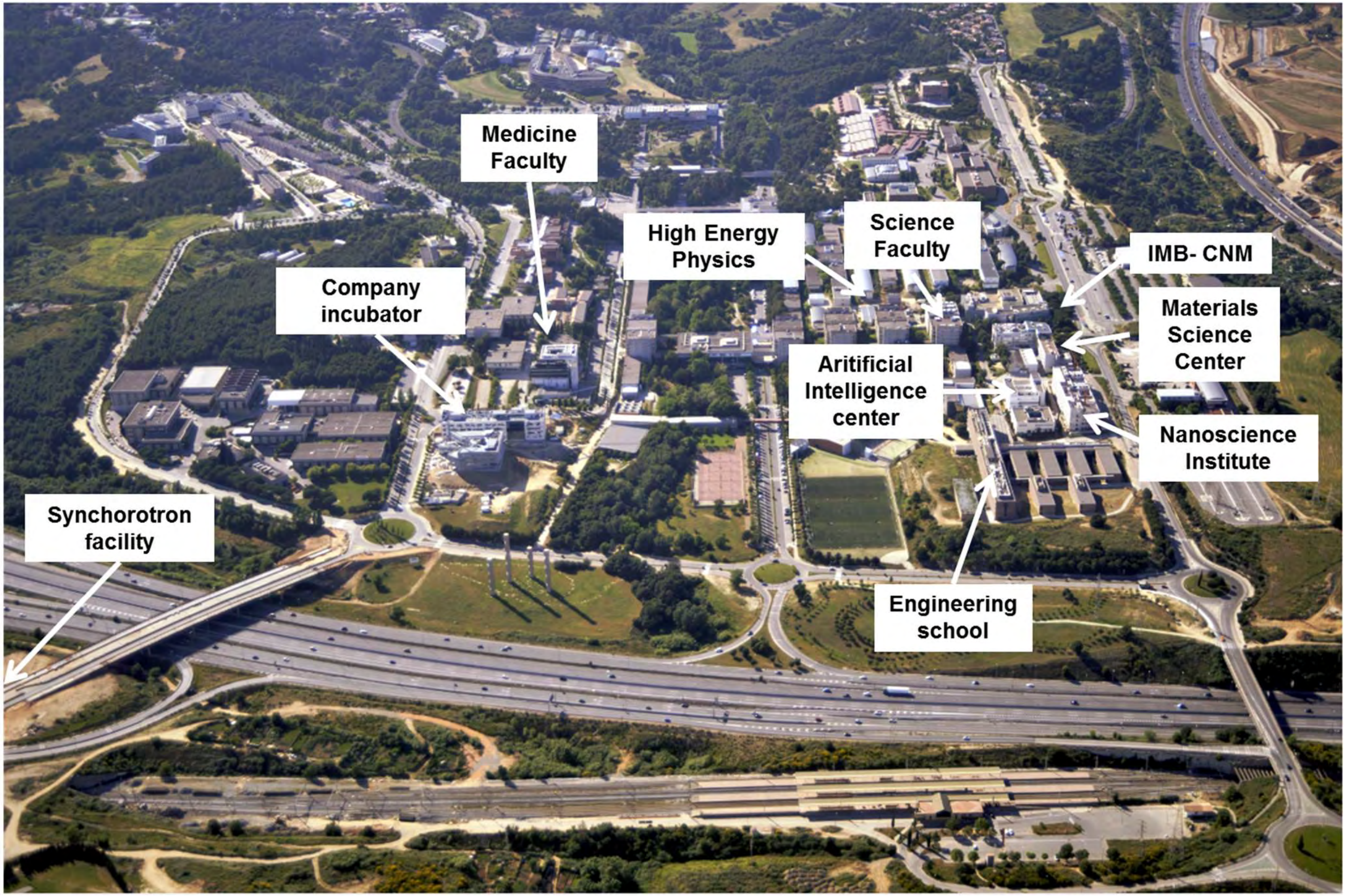
Medicine Faculty
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Company incubator
Materials Science Center
Aritificial Intelligence center
Nanoscience Institute
Synchrotron facility
Engineering school

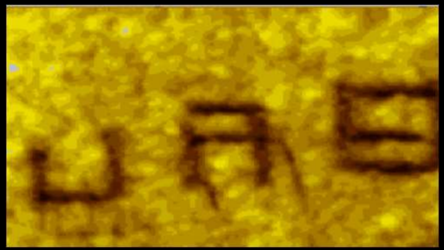
IMB-CNM

Applied research center in the are of micro/nano engineering (Devices, circuits and systems)

200 staff **10** research groups

Micro/Nano fabrication Clean room

1,500 m^2	**40**	**190**	**3000**
total area	staff	equipment units	Wafers/year



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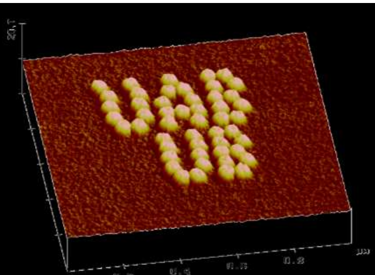
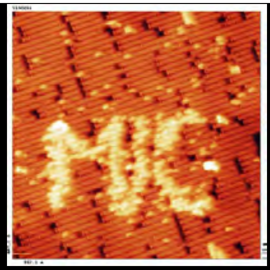


Gorostiza, Servat, Fausto Sanz



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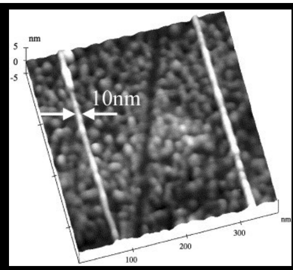

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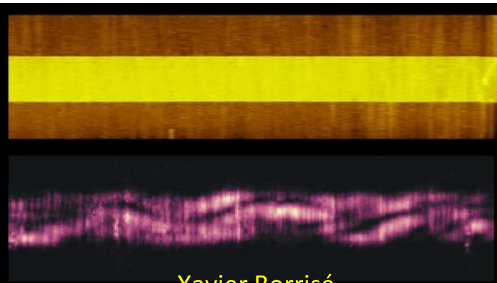

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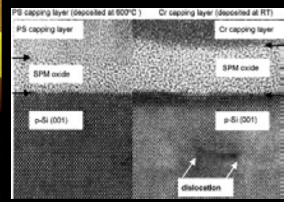

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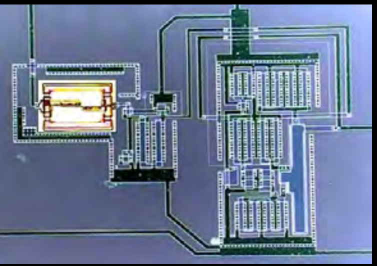
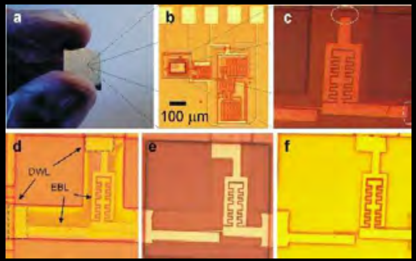
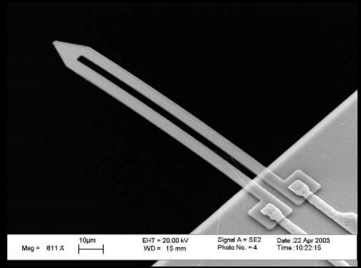


Jaume Verd, Abadal, Barniol



Abadal, Barniol, Boisen



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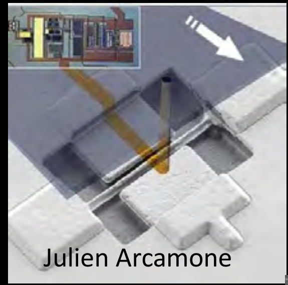

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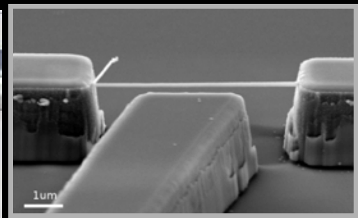

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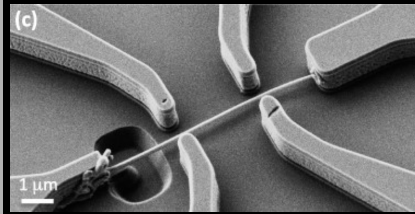

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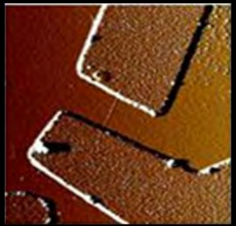
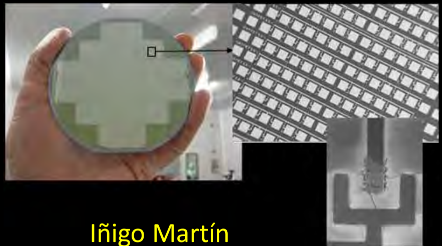


Gemma Rius



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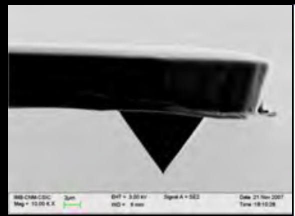

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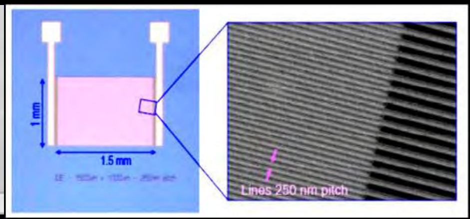

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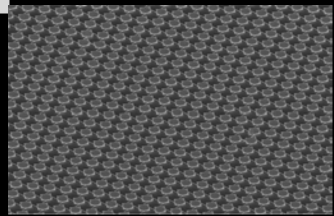

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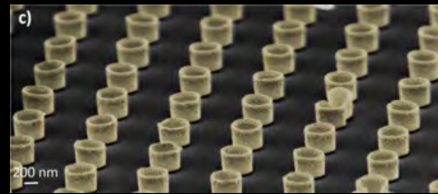

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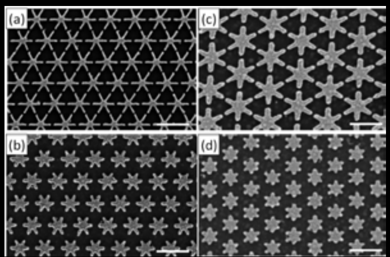
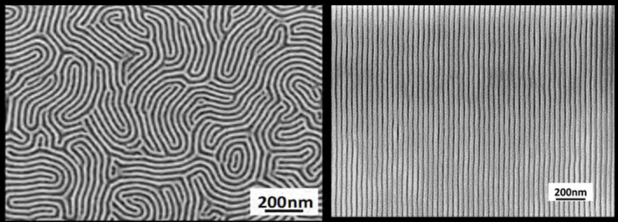
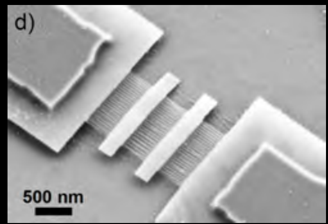


Ana Conde



Lora Oria, Laura Evangelio, Marta Fernandez-Regulez, Steven Gottlieb



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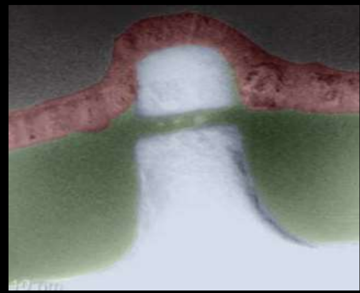
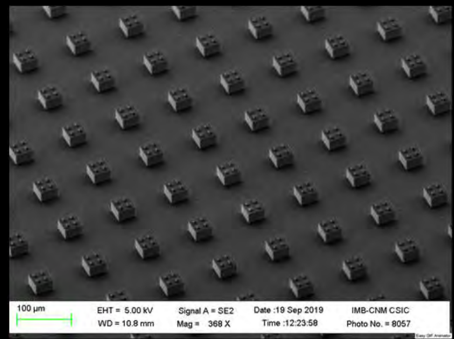


Alberto del Moral, Esteve Amat



Olga Muntada

STRUCTURE

A. Limits of lithography. Recap on principles and limitations

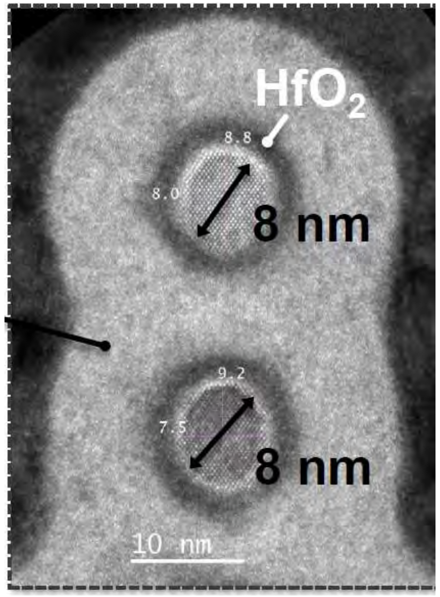
B. Optical lithography. Principles and state of the art

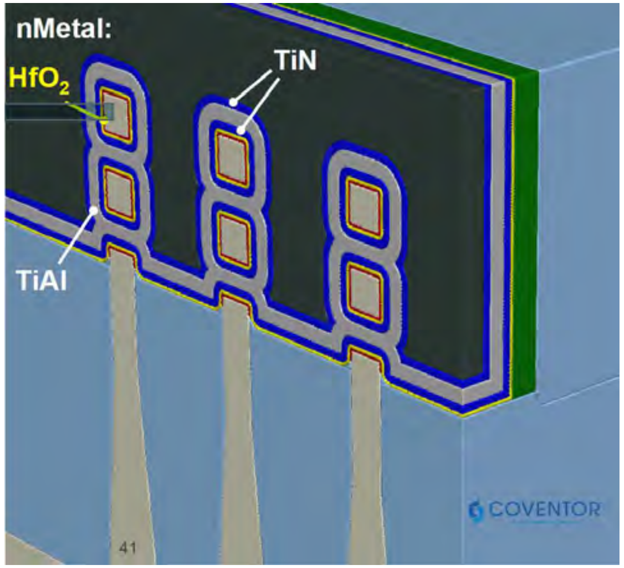
C. Electron and ion beam lithography. Principles and limitation

D. Directed self-assembly (DSA). Concept, principles and relevant examples

The goal is to answer:

- Is there a need for introducing bottom-up methods in advanced lithography





Hans Mertens. Imec. SemiconEuropa, TechArena, Advanced Materials Session, 15/11/2017

Recommended bibliography

Nanofabrication

Nanolithography techniques and their applications

Edited by JoséMaría De Teresa

ISBN 978-0-7503-2608-7 (ebook)

ISBN 978-0-7503-2606-3 (print)

ISBN 978-0-7503-2609-4 (myPrint)

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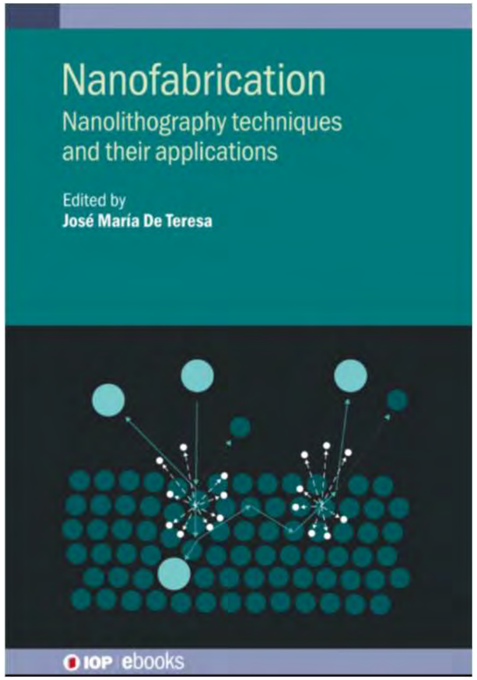
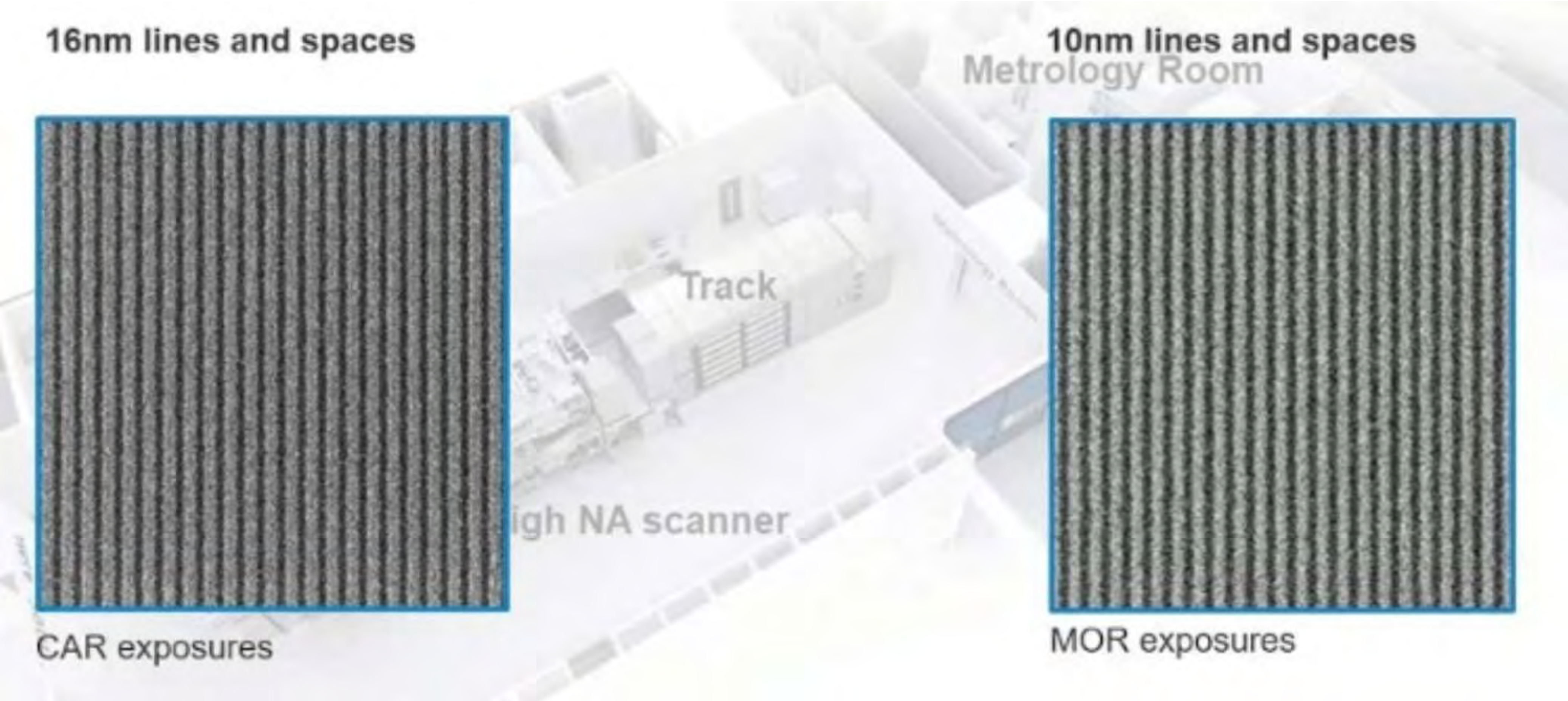


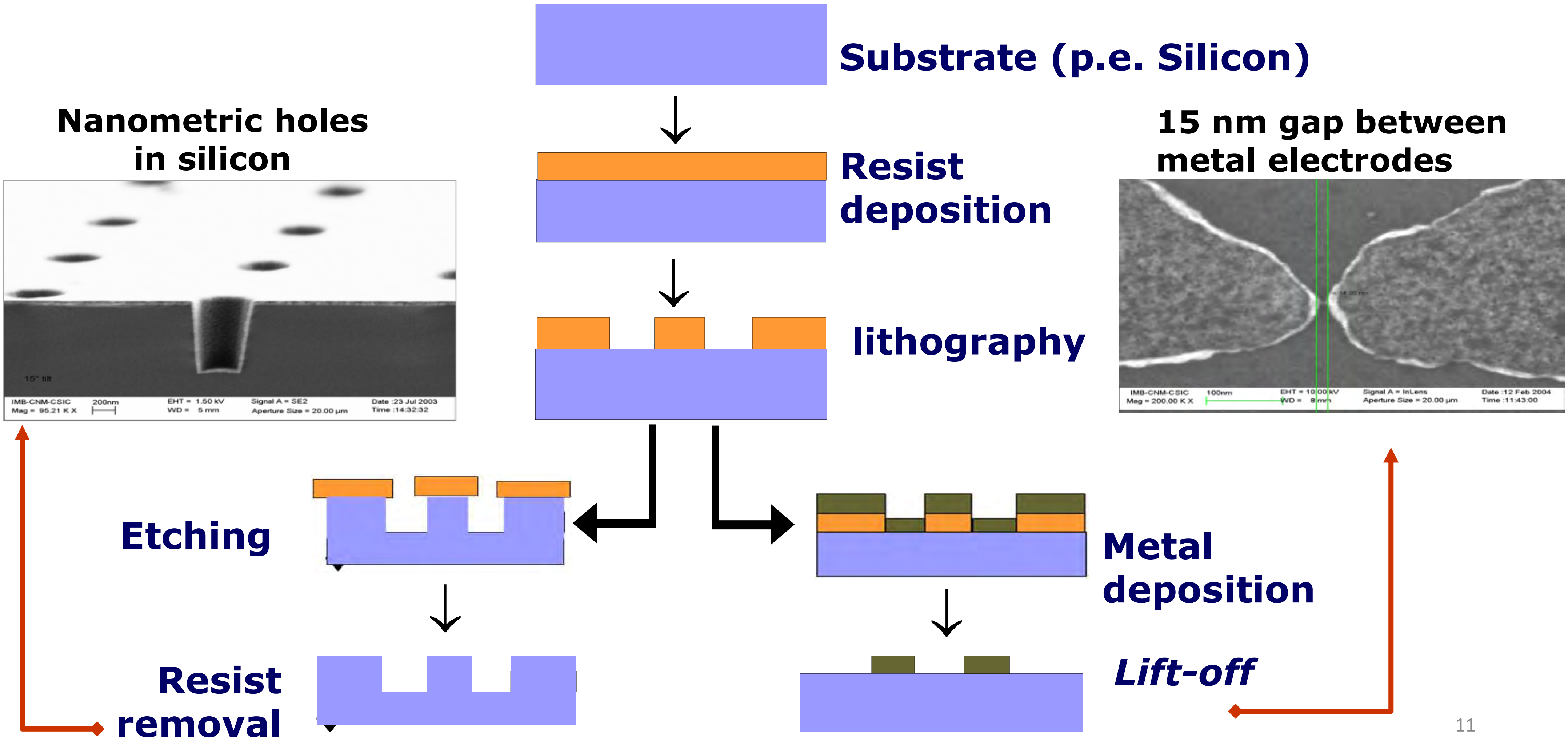
- J. E. E. Baglin, "Ion beam enabled nanoscale fabrication, surface patterning, and self-assembly" Applied Physics Reviews 7, 011601 (2020). https://doi.org/10.1063/1.5143650
- P. Li, et al. "Recent advances in focused ion beam nanofabrication for nanostructures and devices: fundamentals and applications," Nanoscale 13, 1529–1565 (2021), http://dx.doi.org/10.1039/D0NR07539F
- Ji S, Wan et al. Directed self-assembly of block copolymers on chemical patterns: A platform for nanofabrication Prog. Polym. Sci. 54–55 76–127 (2016) ttps://doi.org/10.1016/j.progpolymsci.2015.10.006

A. Limits of lithography. Recap on principles and limitations



https://www.imec-int.com/en/articles/entering-high-na-euv-lithography-era

Lithography based fabrication (top-down)



Main figures of merit in lithography

Resolution: Minimum feature that can be printed in the resist

Throughput: Maximum area that can be printed in a fixed amount of time

Multiple level lithography / alignment: Sequential lithography steps (with other processes in between). The alignment refers to the placement accuracy of a lithography step with respect to the previous one

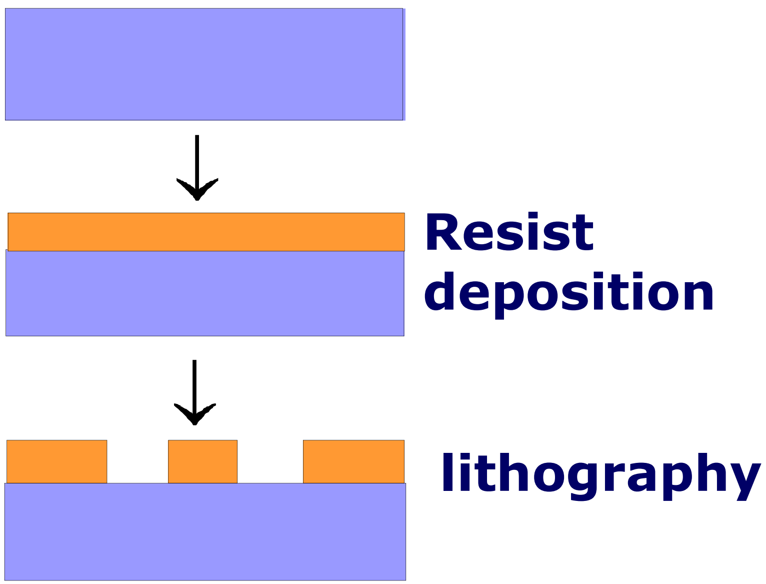
Defectivity: number of relevant defects per area

Pattern fidelity: how close is the obtained pattern to the expected one

Cost of ownership: Lithography costs taking into account several components: equipment, facilities consumables, masks, yield, metrology, maintenance, development….

Resolution:

Minimum feature that can be printed in the resist.



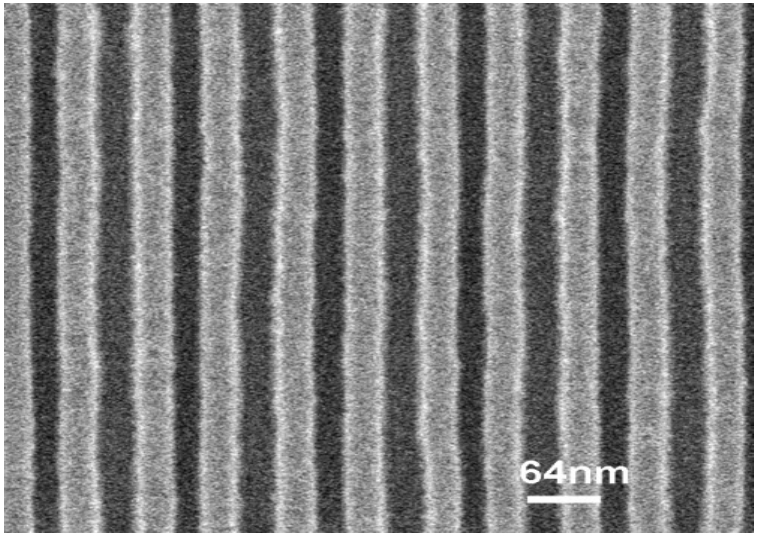
Resolution is the main figure of merit to describe the performance of lithography

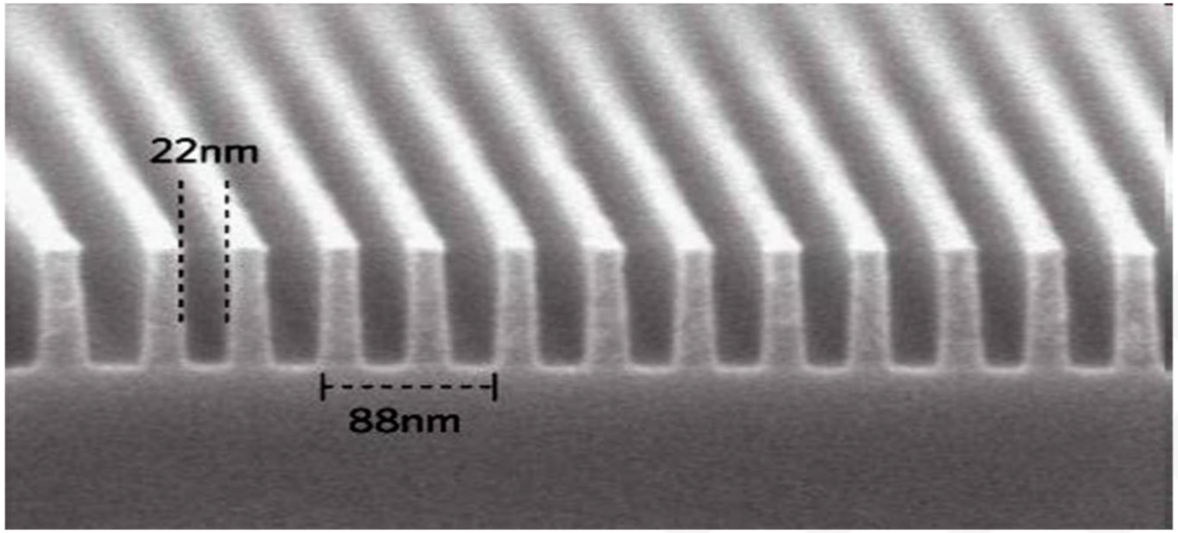
Resolution is defined as the minimum feature that can be printed in the resist

Improving resolution without degrading other parameters (throughput, reliability, etc) has been the battle horse of nanofabrication

Resolution:

Minimum feature that can be printed in the resist.

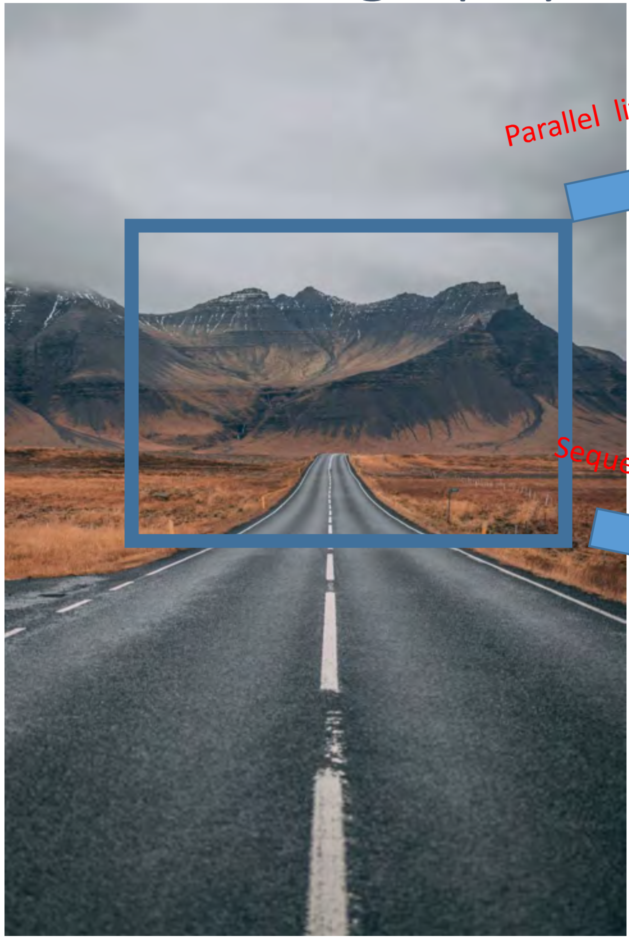




Usually resolution is defined for dense /periodic patterns:
Minium **half pitch** (half period) achievable

Throughput

Parallel vs sequential Lithography



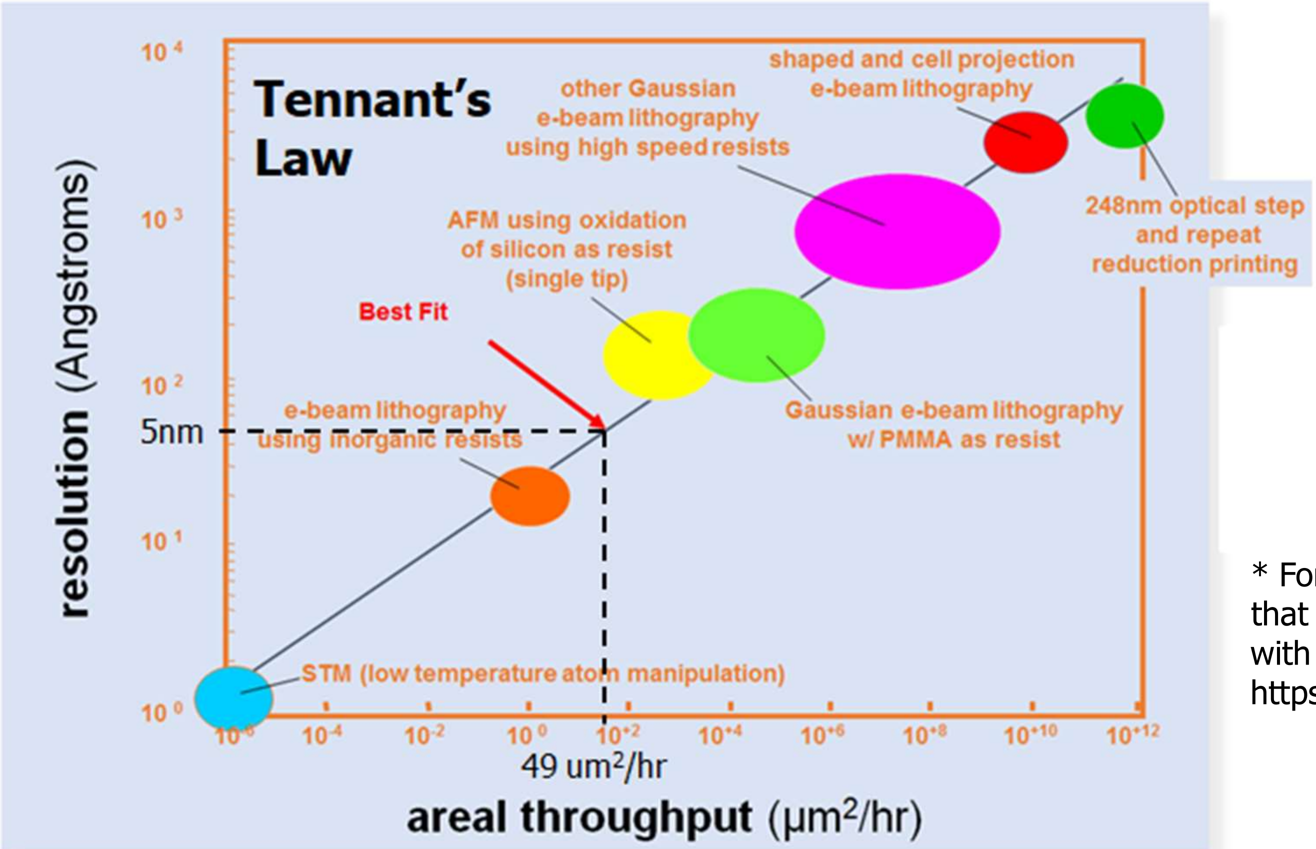
Parallel lithography

Less than 1 second

Sequential lithography

More than 1 hour

Resolution vs Throughput

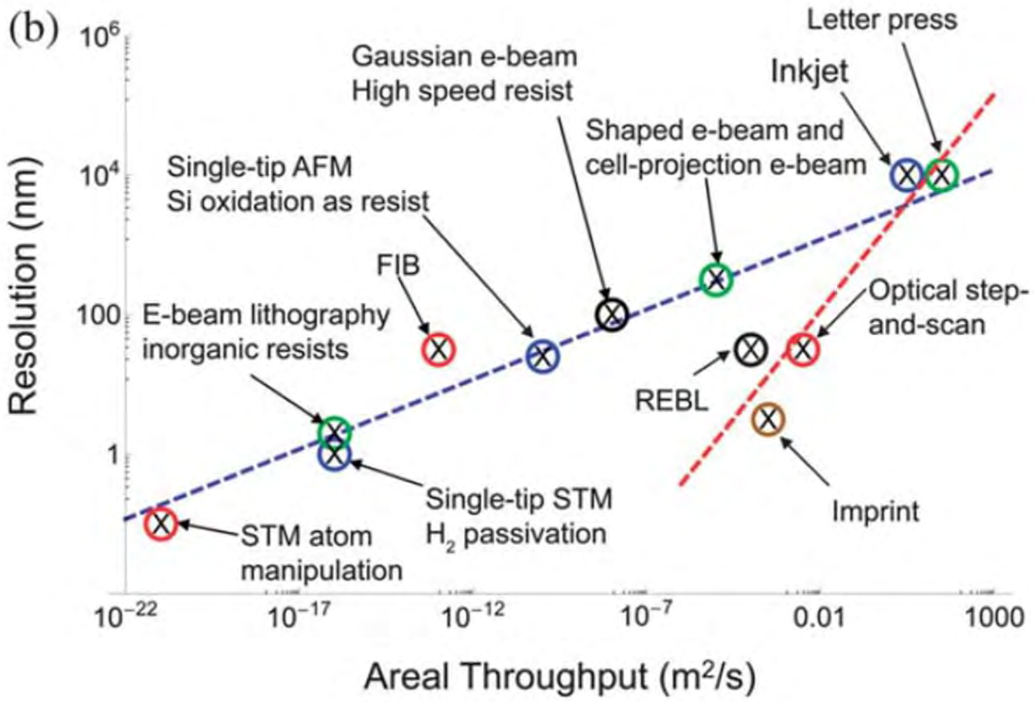


D. M. Tennant, Nanotechnology, edited by G. Timp (Springer-Verlag, New York, 1999), p.164

Throughput (μm²/hour) = (resolution[nm]/2.3)⁵

* For an excellent discussion of Tennant's Law and the reason that throughput for direct write tools has a 5th order relationship with resolution, see https://www.lithoguru.com/scientist/essays/Tennants_Law.html

Resolution vs Throughput



Updated resolution vs throughput graph
(from Liddle and Gallatin. Nanoscale 3, 2679 (2011)).

Why $A_t = k_T R^5$?

- Serial patterning:
  - $A_t \sim R^2$
    Higher resolution implies smaller pixel size, and so more pixels to expose
  - $A_t \sim R^3$
    Writing a small pixel takes much longer than writing a big pixel
    - Sensitivity of the photoresist goes down as the resolution improves
    - Greater precision is required when resolution decreases
    - Avoid stochasticity

- Parallel patterning:
  - $A_t \sim R^2$ does not apply (all pixels patterned at the same time)
  - $A_t \sim R^3$ (even smaller due to improves in instrumentation)

Defectivity: number of relevant defects per area

For advanced technology nodes, such as 7nm, 5nm,and below, the maximum defectivity levels are expected to be in the range of:

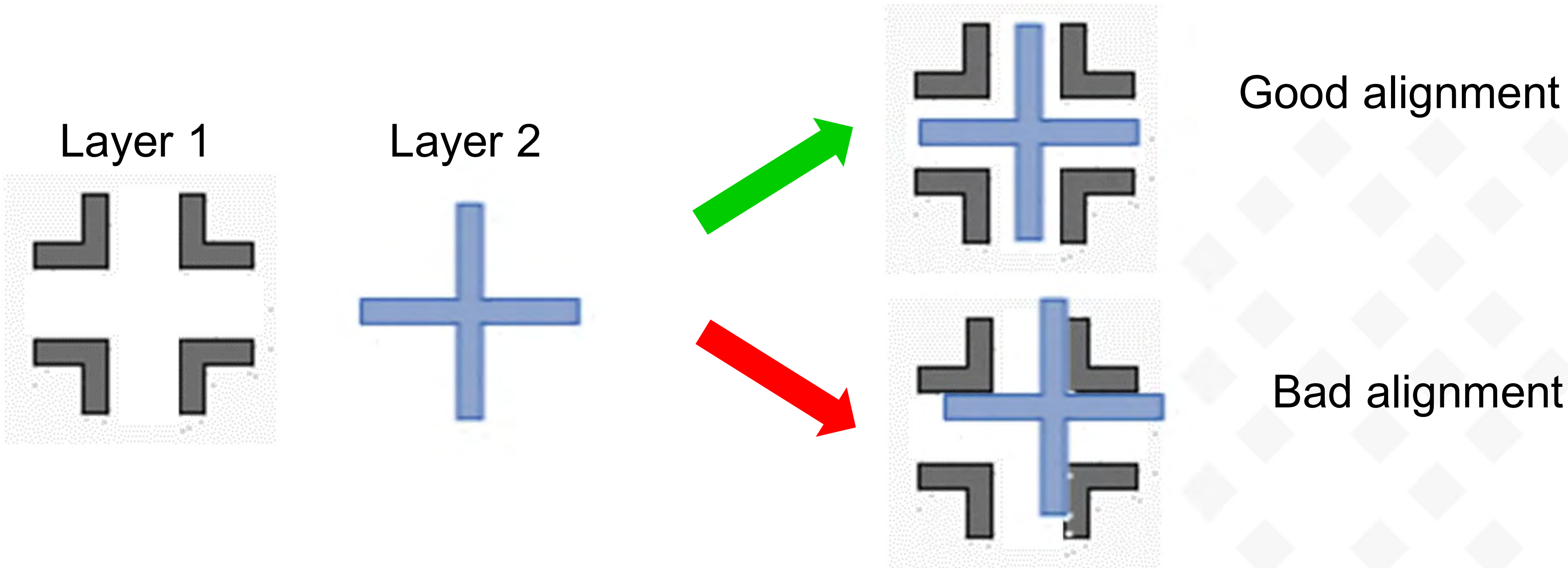
1 defect per square centimeter (1 defect/cm^2) or lower for critical layers.

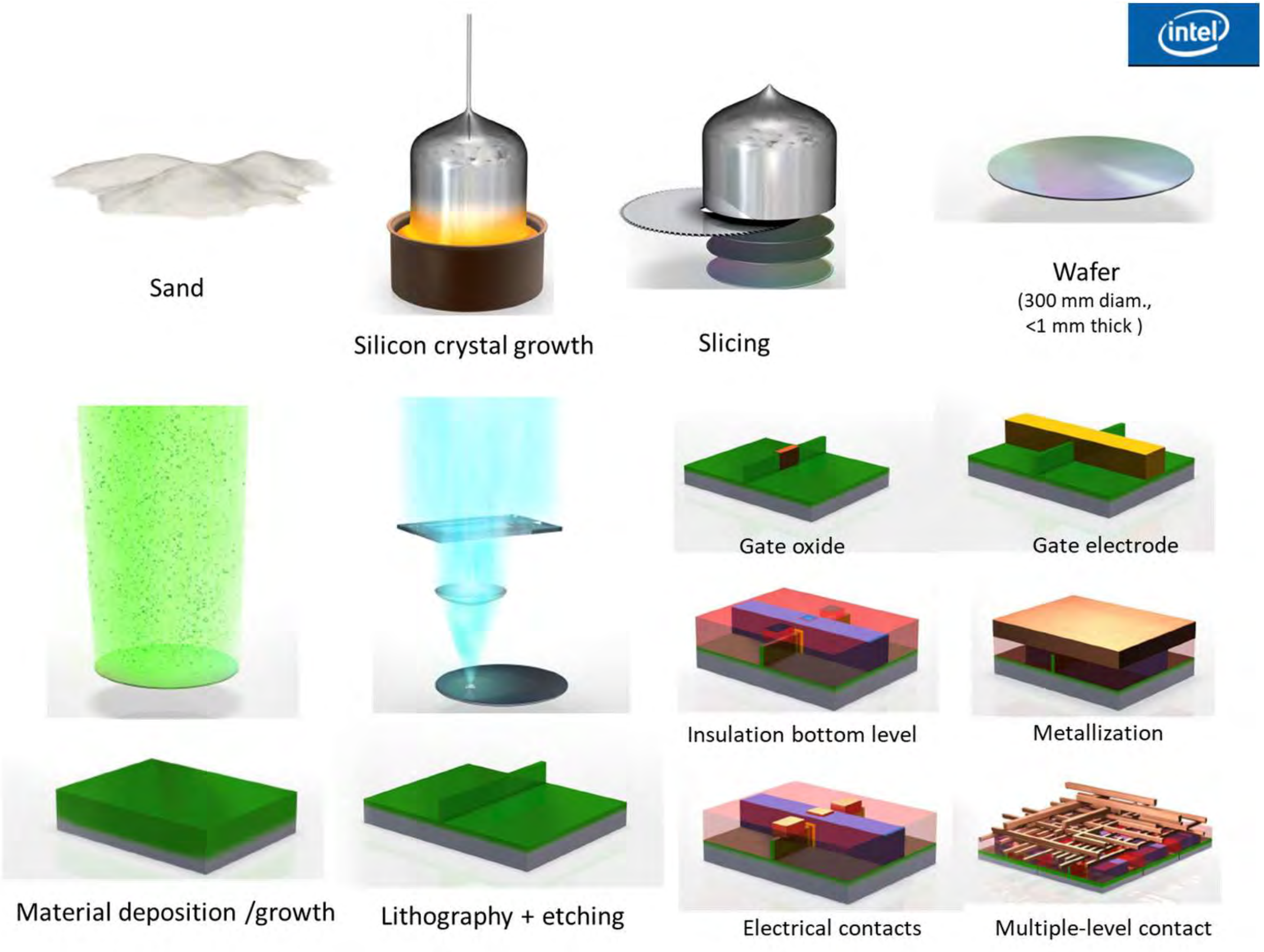
Defects can appear due to:

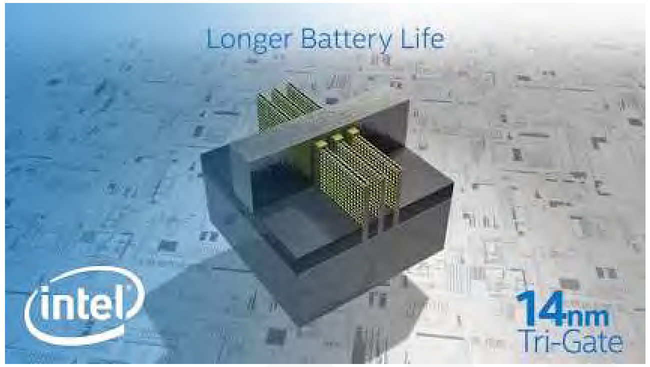
- Impurities in the materials
- Contamination
- Processing limitation
- Stochasticity

Multiple level lithography / overlay alignment:

Sequential lithography steps (with other processes in between).
The alignment refers to the placement accuracy of a lithography step with respect to the previous one

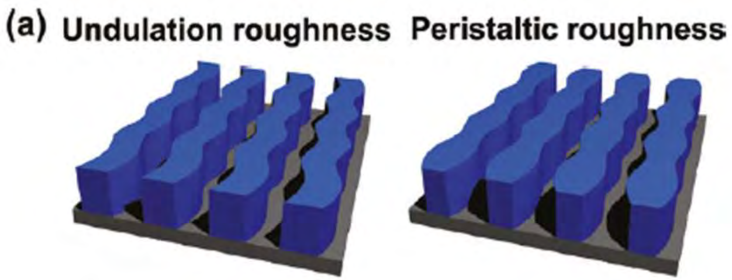


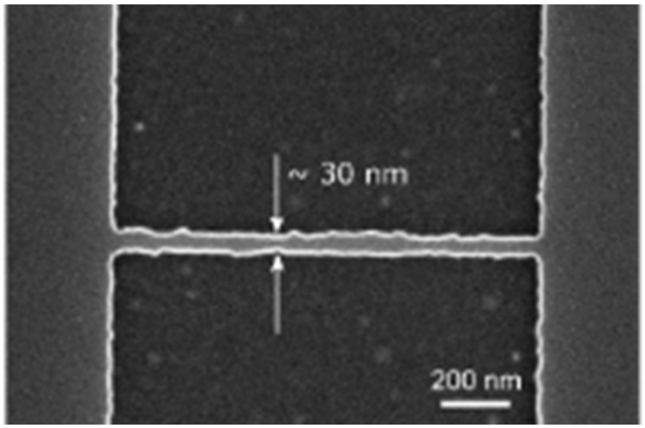

Sand
Silicon crystal growth
Slicing
Wafer
(300 mm diam.,
<1 mm thick)
Gate oxide
Gate electrode
Insulation bottom level
Metallization
Material deposition /growth
Lithography + etching
Electrical contacts
Multiple-level contact


Longer Battery Life
14nm
Tri-Gate

Pattern transfer fidelity

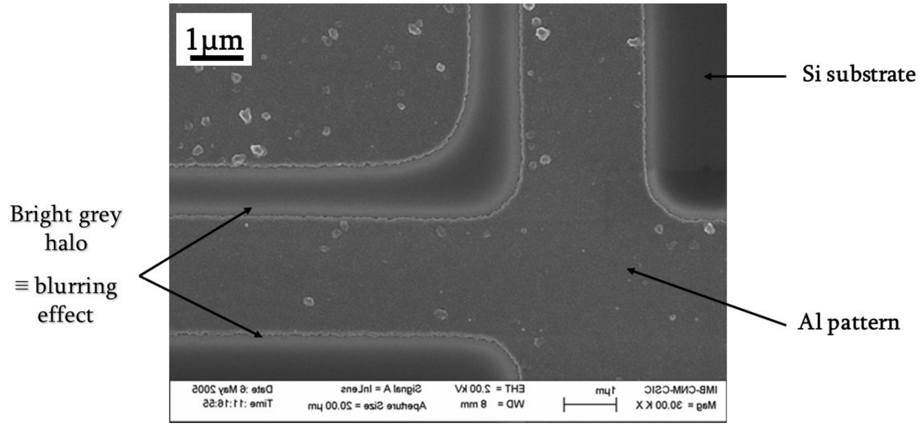
- Line Edge Roughness (LER) is the roughness or deviation in the position of an edge as a function of distance along the edge



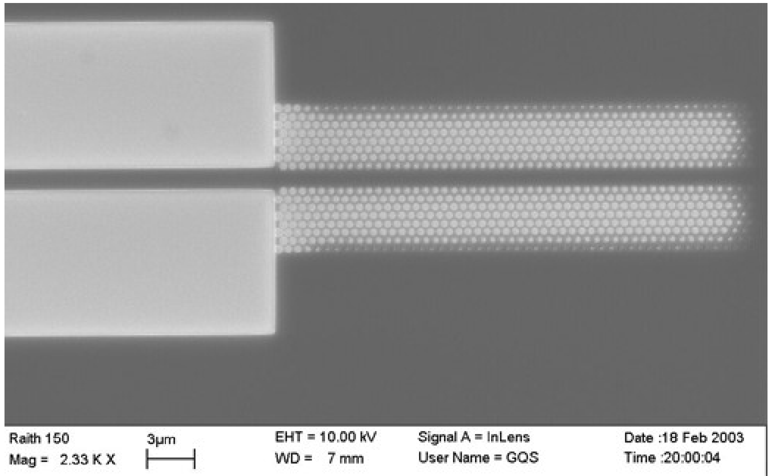


- Blurring

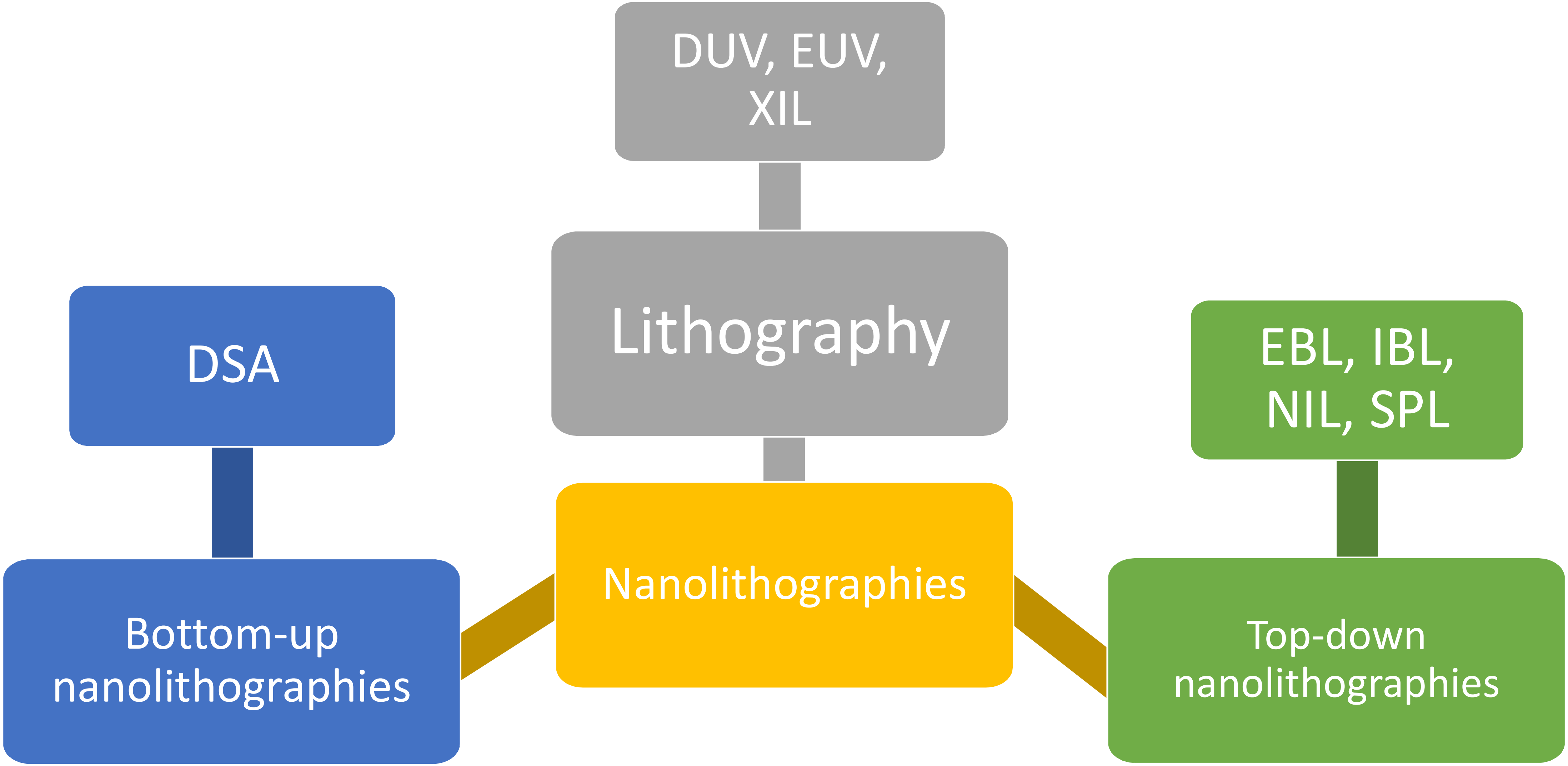
Step 1: Nanostencil-based deposition of Al (70 nm thick) on Si



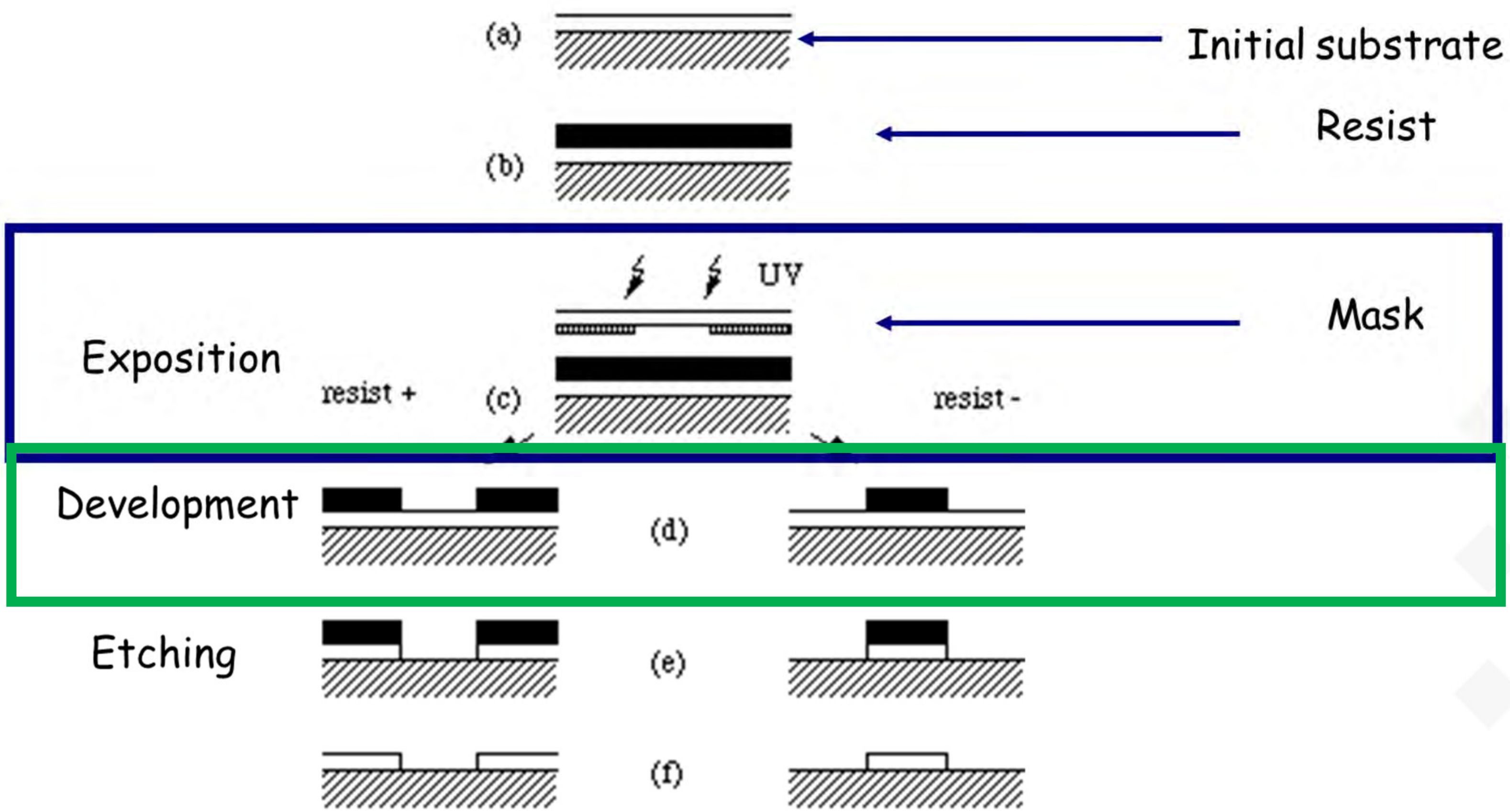
- Non uniformity

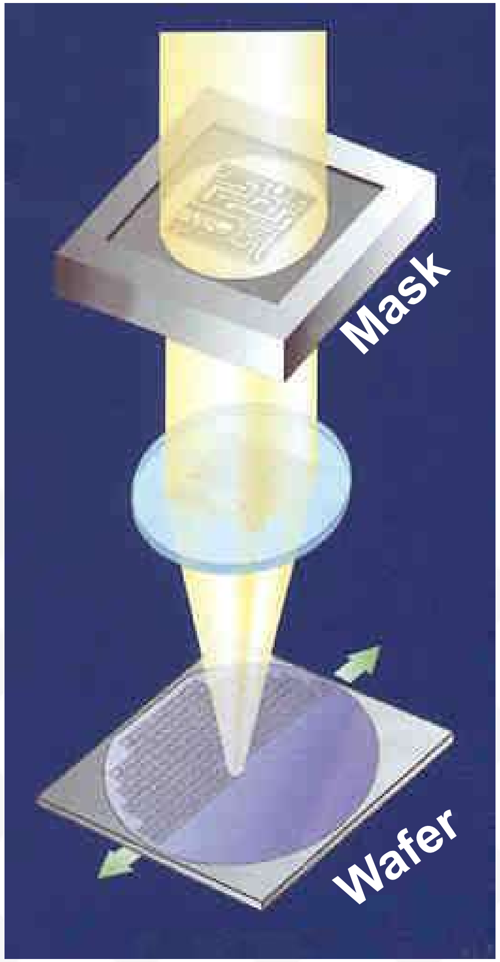


Lithographies



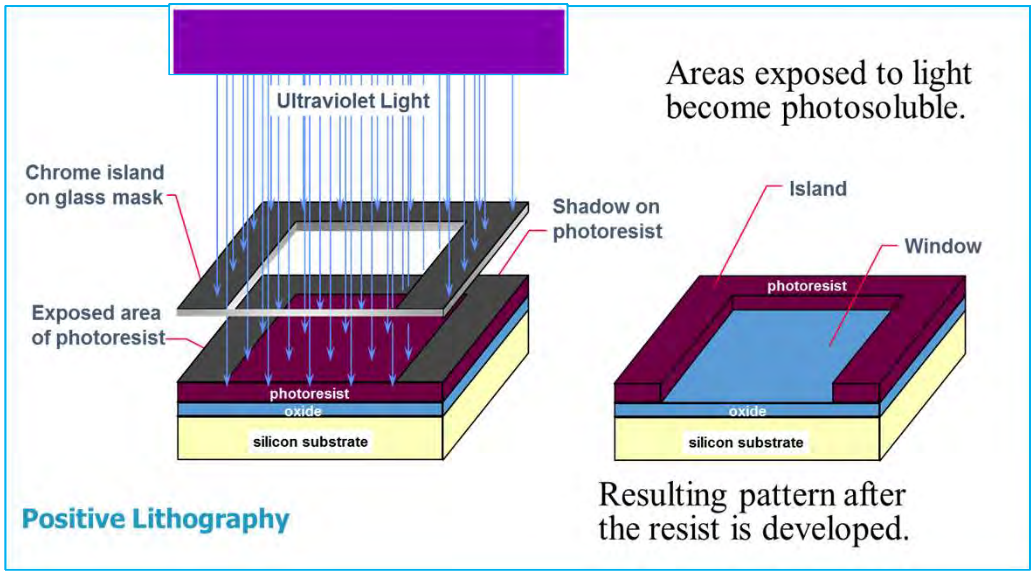
Fabrication using optical lithography



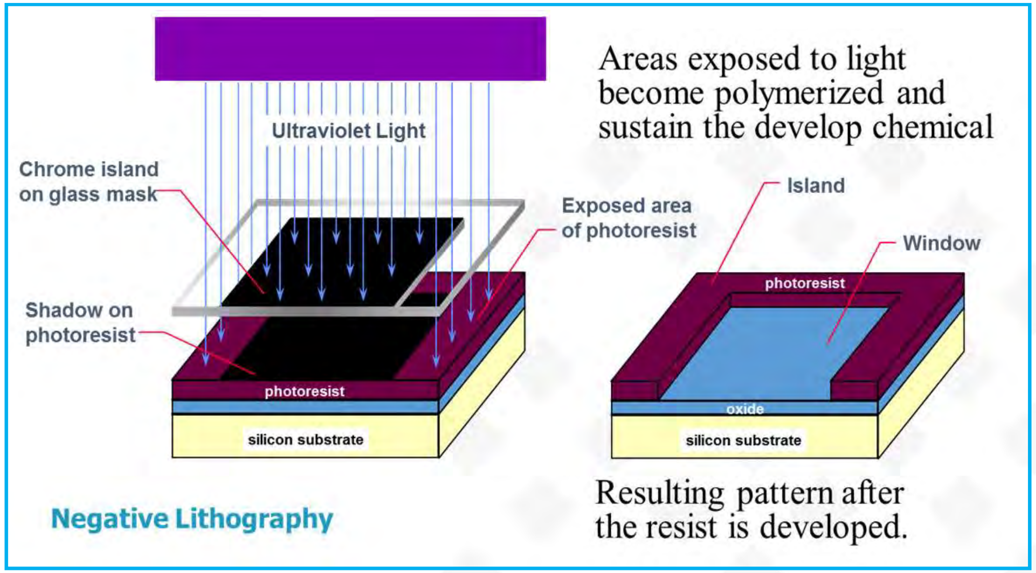


Positive and negative resists

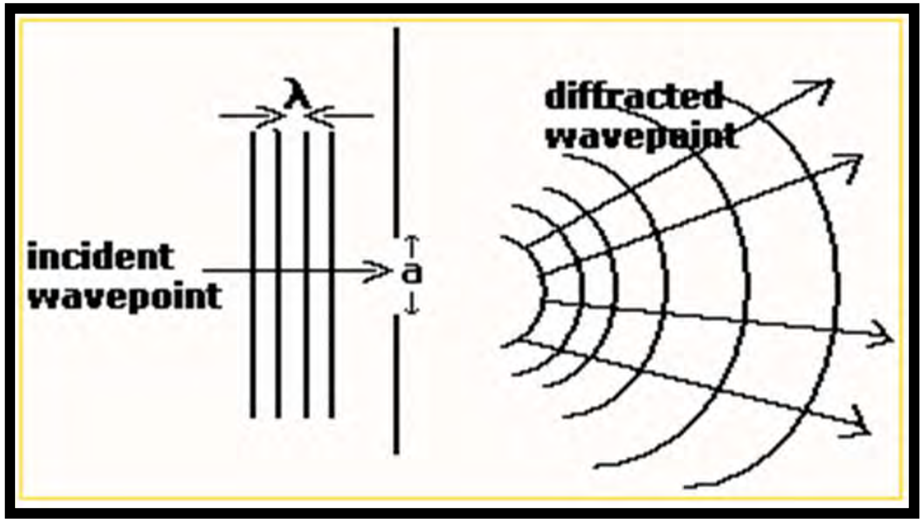
Positive resist

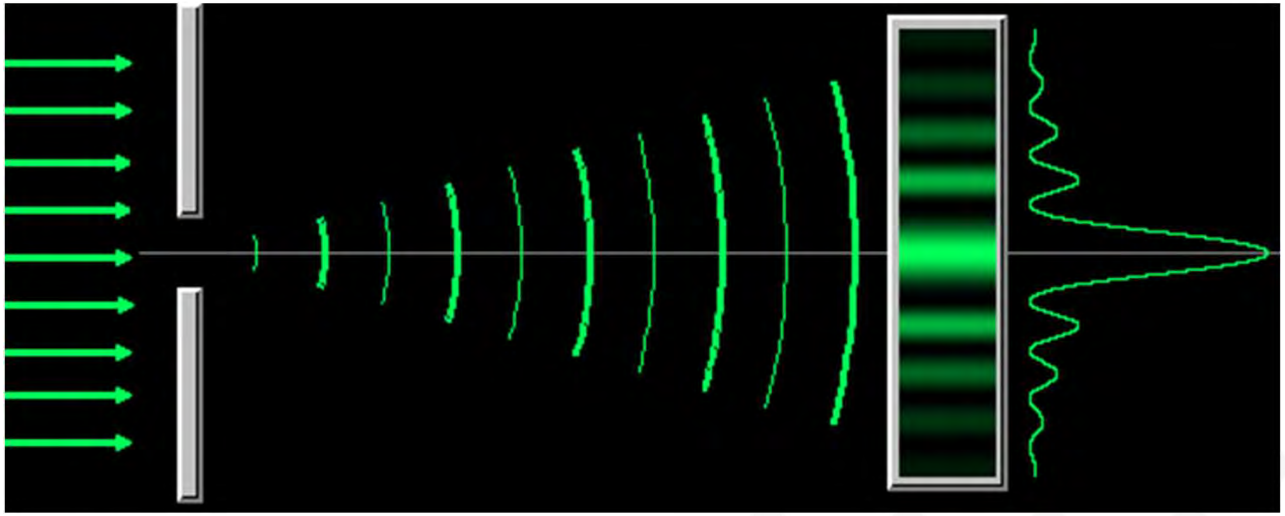


Negative resist



Resolution is limited by diffraction in optical lithography



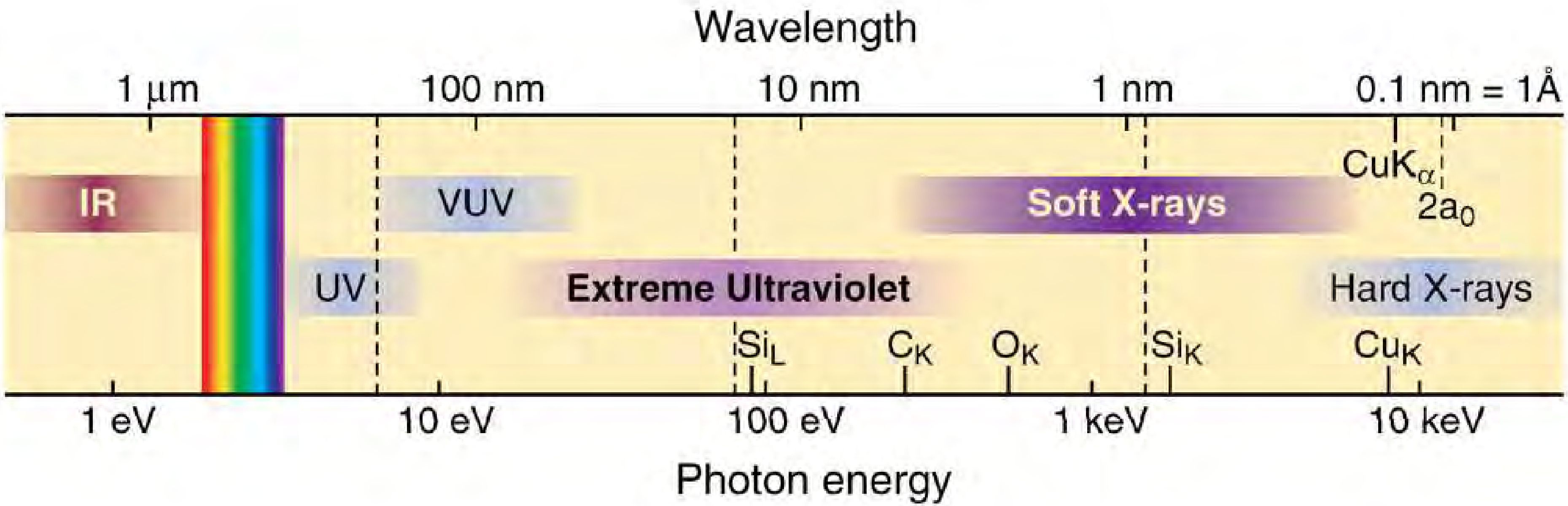


The effect of diffraction is specially relevant when th slit aperture is similar to the wavelength of the radiation

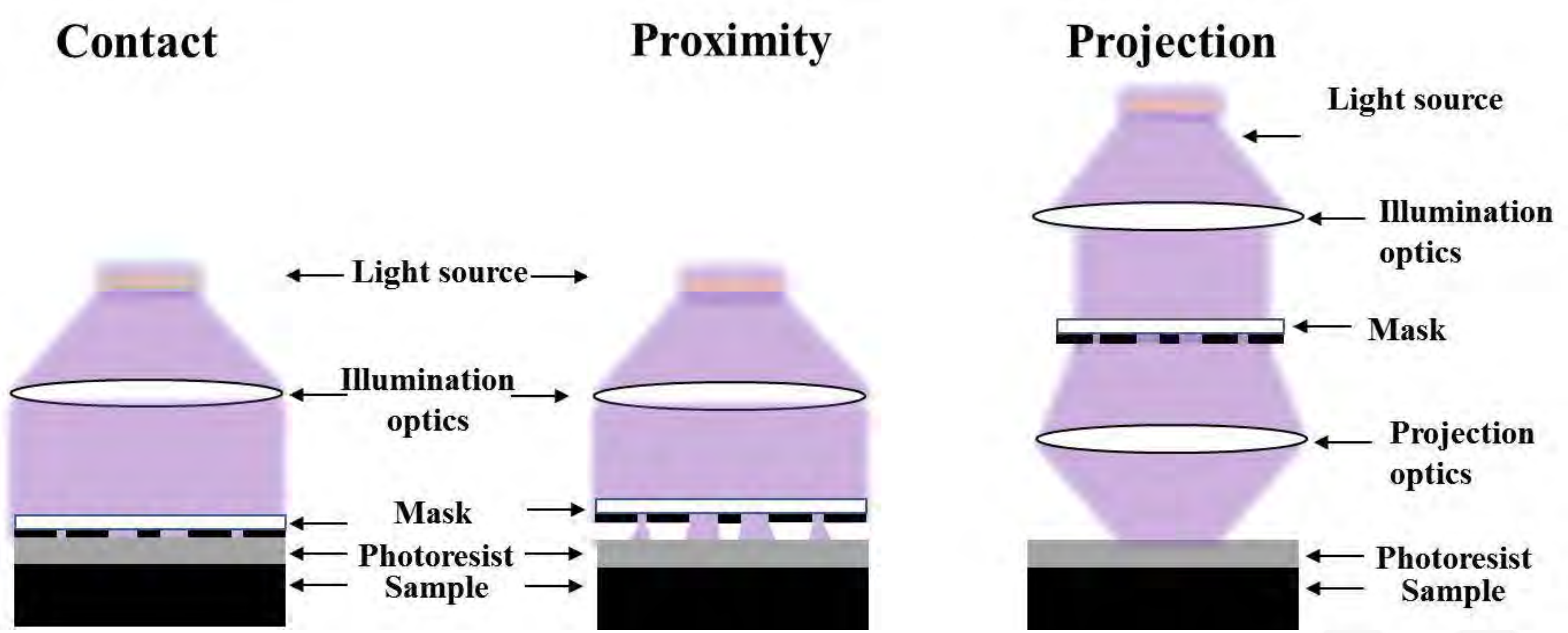
$(a \sim \lambda)$

Optical radiation

Electromagnetic spectrum, from the infrared (longer wavelengths)) to x-rays higher wavelengths



Optical lithography modes

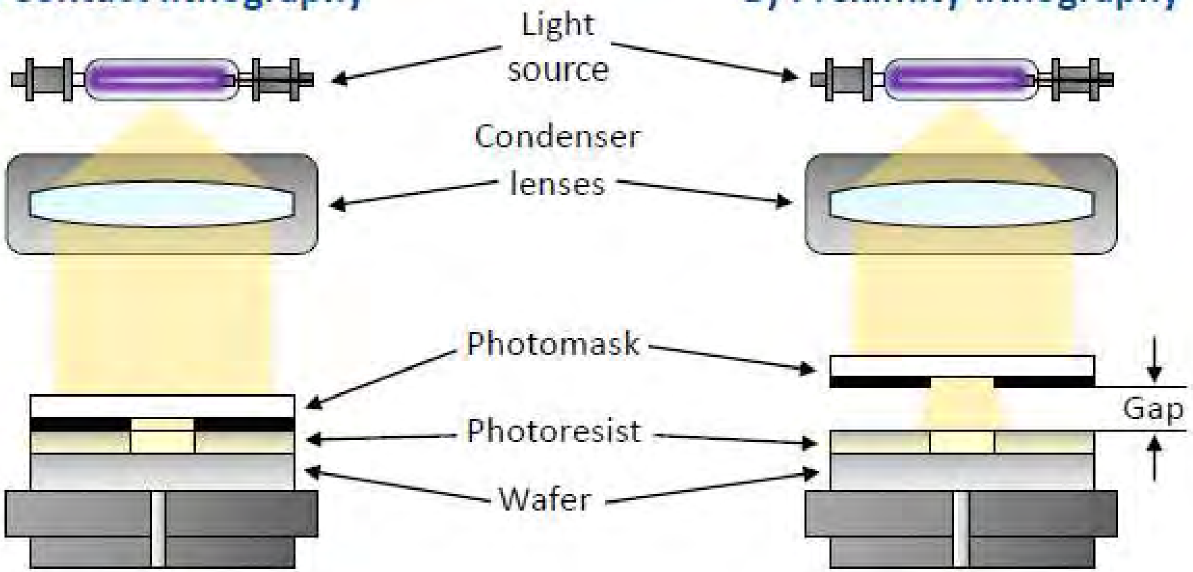


Magnification factor	1:1	1:1	5:1	Magnification factor

Optical lithography modes (Summary)

A) Contact lithography

B) Proximity lithography



Photomask in contact with the wafer.

$$\text{Resolution} = \sqrt{\lambda\, d} \approx 0.6\ \mu\text{m}$$

d: Resist thickness (~1 µm)

λ: Wavelength (g, 436 nm)

Photomask separated from the wafer

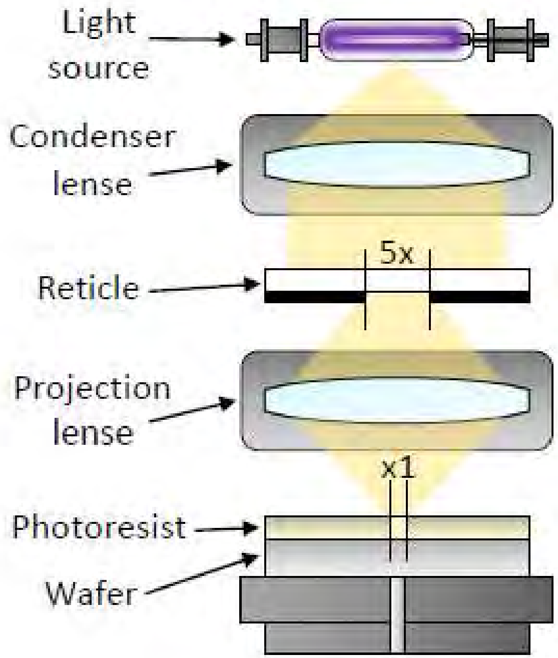
$$\text{Resolution} = k\,\sqrt{\lambda\, g} \approx 3.0\ \mu\text{m}$$

g: Proximity gap (~20 µm)

λ: Wavelength (g, 436 nm)

k: Experimental parameter (> 1 µm)

C) Projection lithography



Reduction between 5–10x
Exposure step-by-step

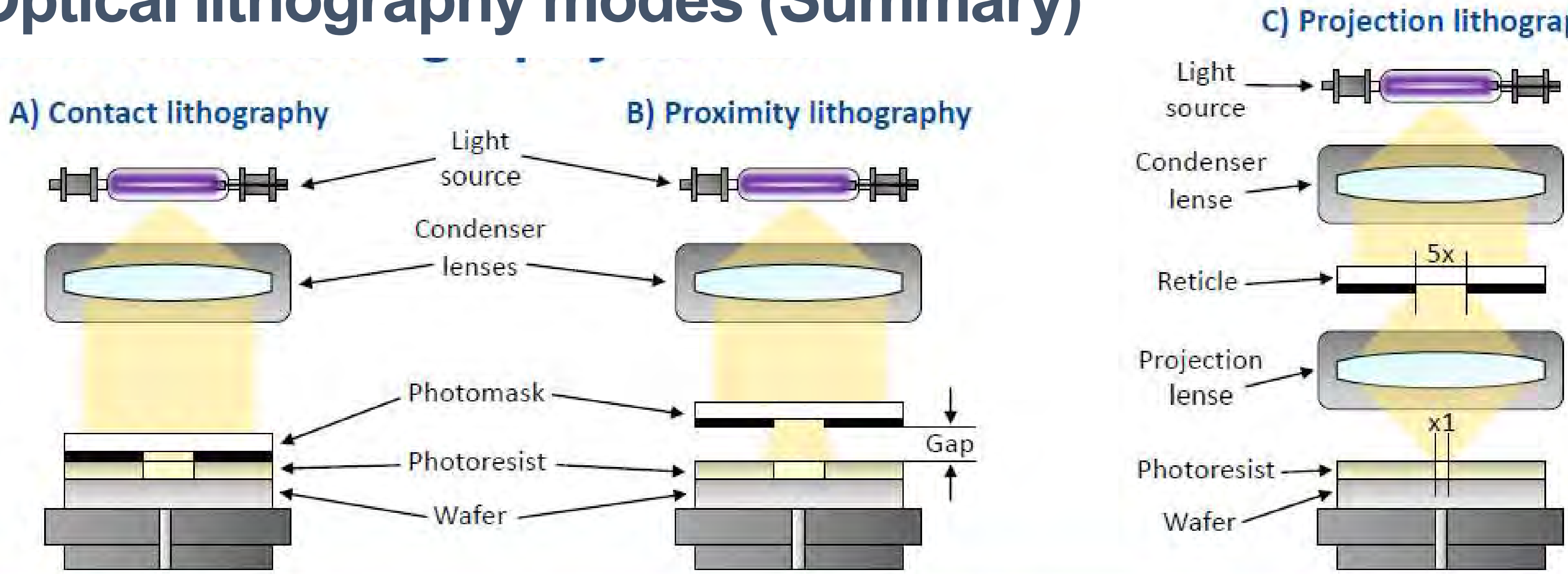
$$\text{Resolution} = k_1 \frac{\lambda}{NA} \approx\ 0.4\ \mu\text{m}$$

NA: Numerical aperture (~0.7)

λ: Wavelength (g, 436 nm)

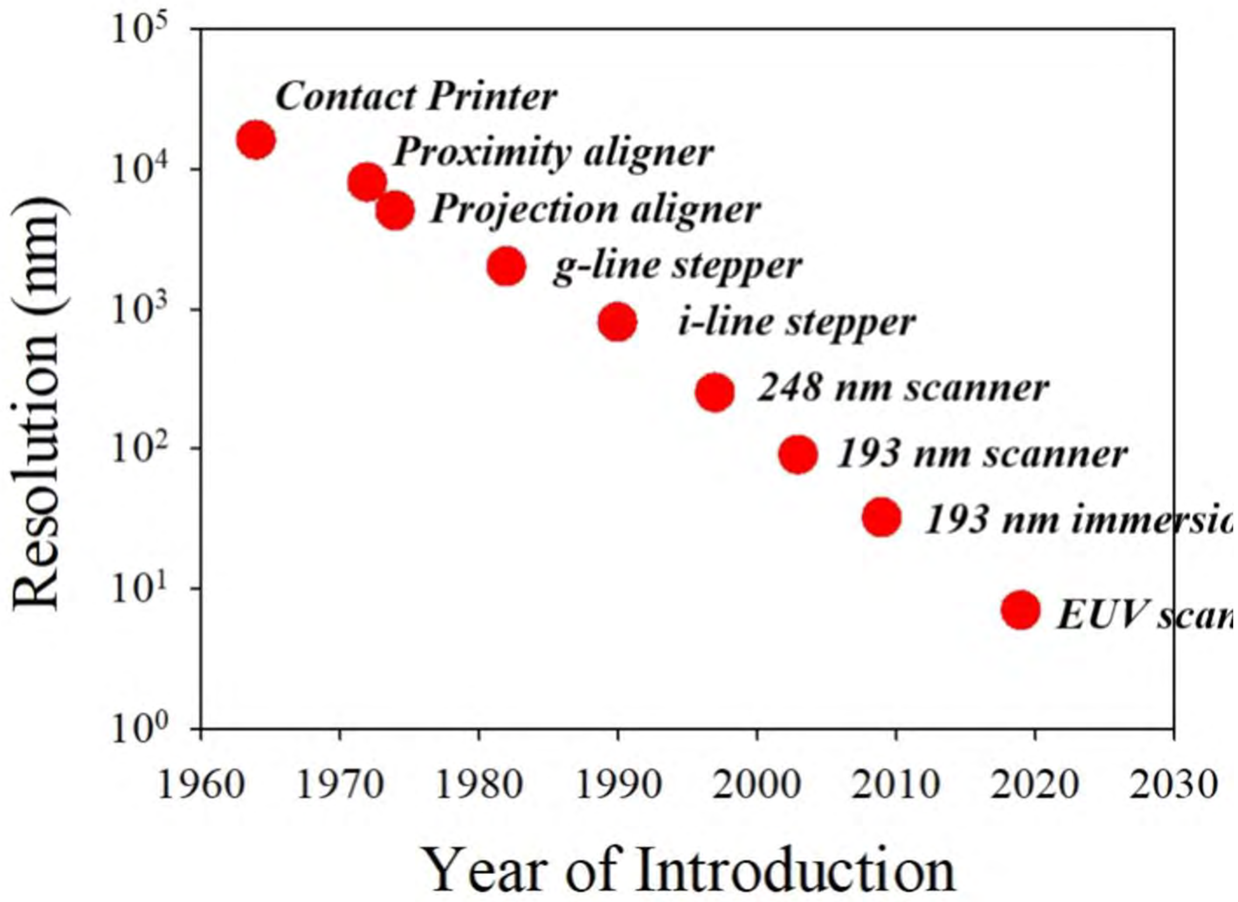
k_1: Technology constant (0.5 – 0.9)

Optical lithography modes (Summary)



A. Contact	Each contact may induce defects on the wafer	Requires constant photomask cleaning	Reduced photomask lifetime	If there are particles on the photomask, contact is not good and neither is resolution	Only one level, size and distribution per mask	A local defect on the photomask causes a local defect on the wafer	Higher resolution (in absence of particles) than proximity
B. Proximity	Contact is slightly avoided, so are defects	Requires eventual photomask cleaning	Extended photomask lifetime	Even with some particles, resolution can be ensured	Only one level, size and distribution per mask	A local defect on the photomask causes a local defect on the wafer	Lower resolution than contact
C. Projection	Mask is not in contact, so induced defects are completely avoided	Reticle does not require cleaning	Reticles last forever	If there are particles on the reticle, they are transferred to the photoresist	Several levels and distributions per mask	A local defect on the photomask causes a defect on each die of the wafer	Higher resolution than both contact and proximity

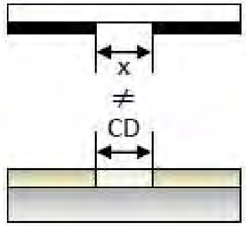
Optical lithography at the nanoscale



Evolution of the optical resolution during the years. Data extracted from Hutcheson G D 2018 Moore's law, lithography, and how optics drive the semiconductor industry Proc. SPIE 1058303 501

State of the art

How to reduce **Critical Dimensions**?

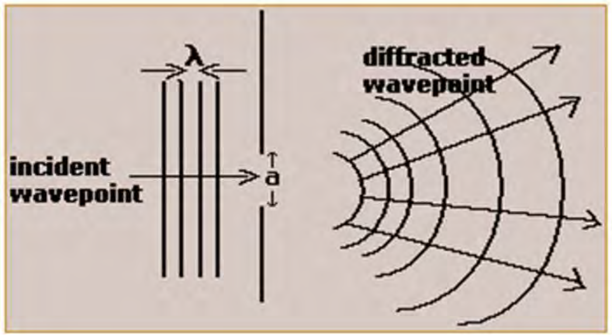


Rayleigh criterion:

$$CD = \kappa_1 \frac{\lambda}{NA}$$

- NA: Numerical aperture
- κ_1 : Technology factor
- λ: Light source wavelength

Diffraction limits resolution

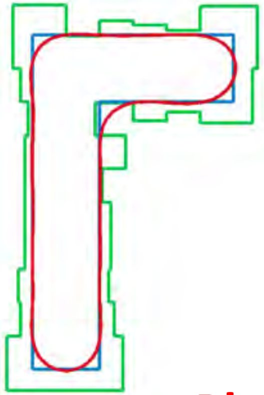


$$R = k1 \frac{\lambda}{NA}$$

K_1=0.22, λ= 193 nm, NA=1.35

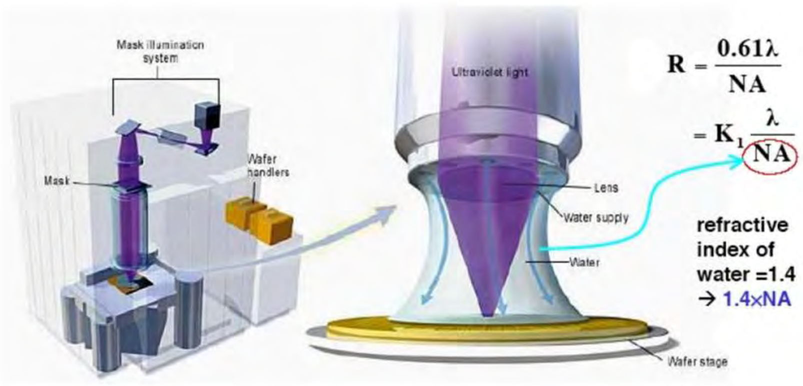
Resolution= 32 nm

Optimal proximity correction



When features of different geometries and sizes exist, correcting for the proximity effects requires adjusting the geometries, what is known as OPC. For complex structures at the limit of resolution, OPC is complex and requires dedicated modelling.

Immersion DUV Lithography



Phase shifting masks

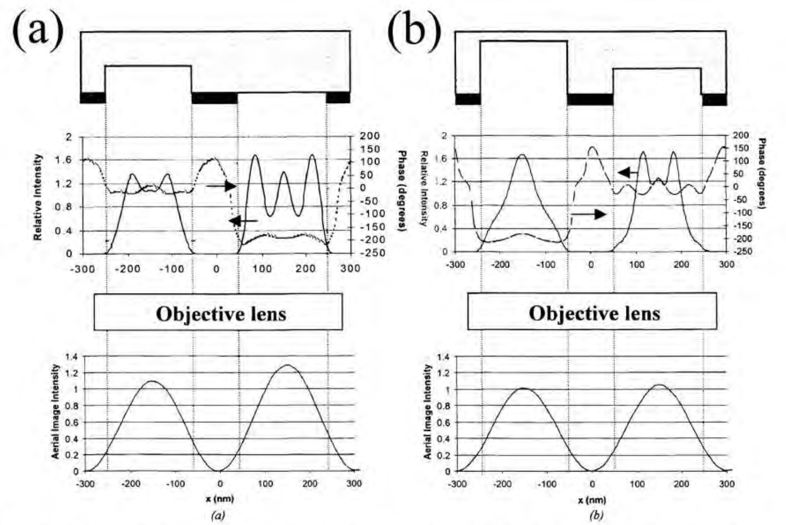
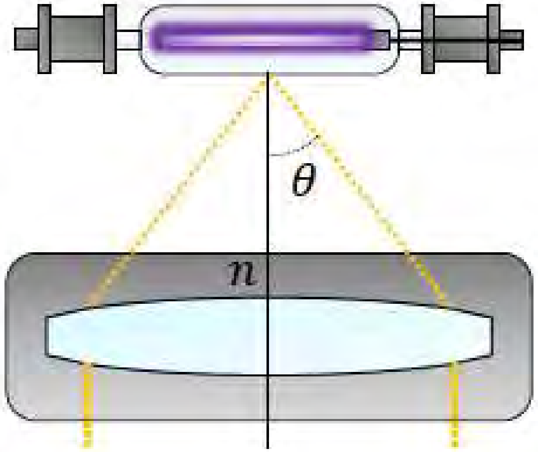


Figure 2.6. Concept of alternating phase shifting mask. Calculation of the in-focus aerial image after passing through a 4X stepper at DUV illumination (248 nm wavelength), and numerical aperture of 0.6 for a simple subtracting alternating phase shifting mask (a) and a dual trench one (b). Figure reproduced from [8], copyright SPIE.

A) Increase the Numerical Aperture

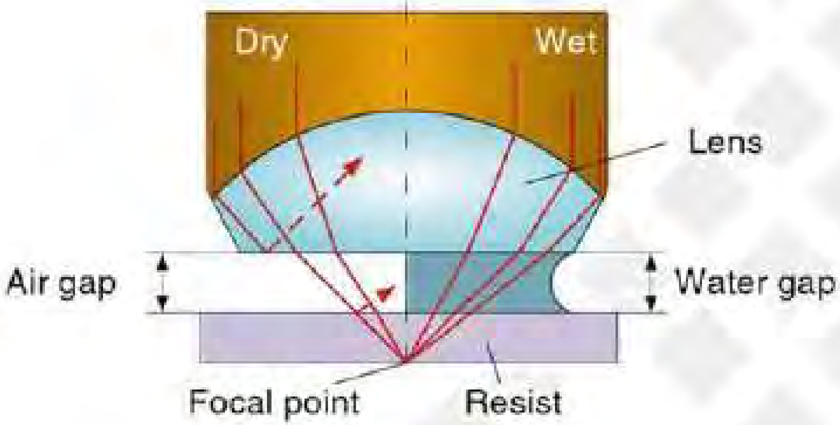
The NA is a property of the lens, a dimensionless number defined by the angular range over which an optical system can accept or emit light.



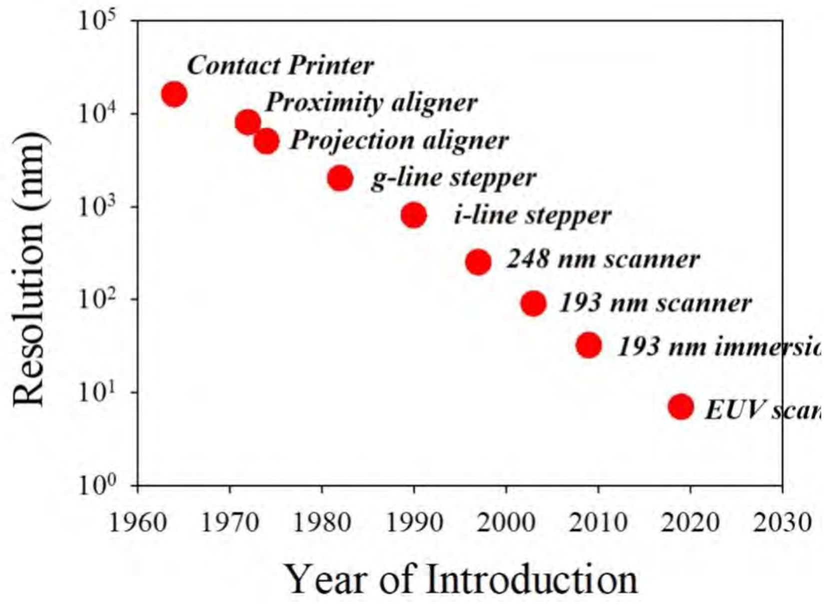
$$NA = n \sin\theta$$

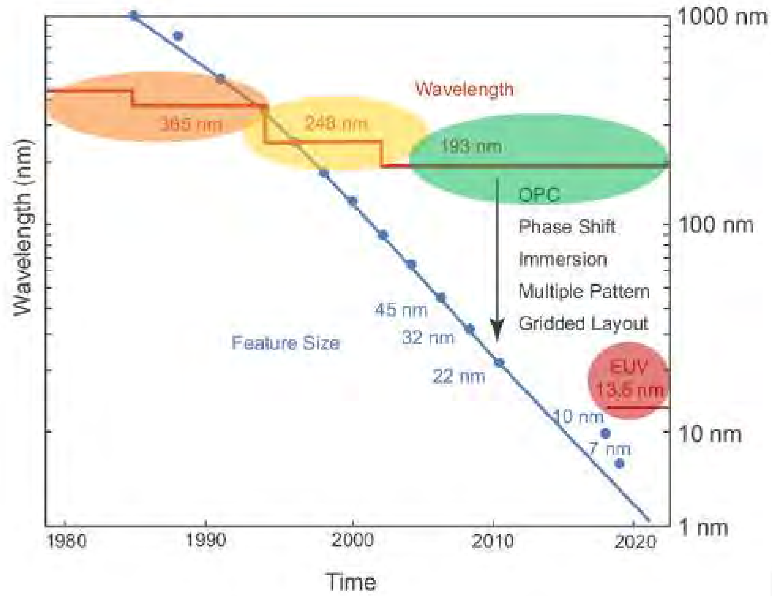
- θ: Maximum half-angle of light through the lens
- n : Index of refraction of media (1.00 for air, 1.33 for pure water)

Immersion lithography



Immersion lens:
(effective) NA > 1

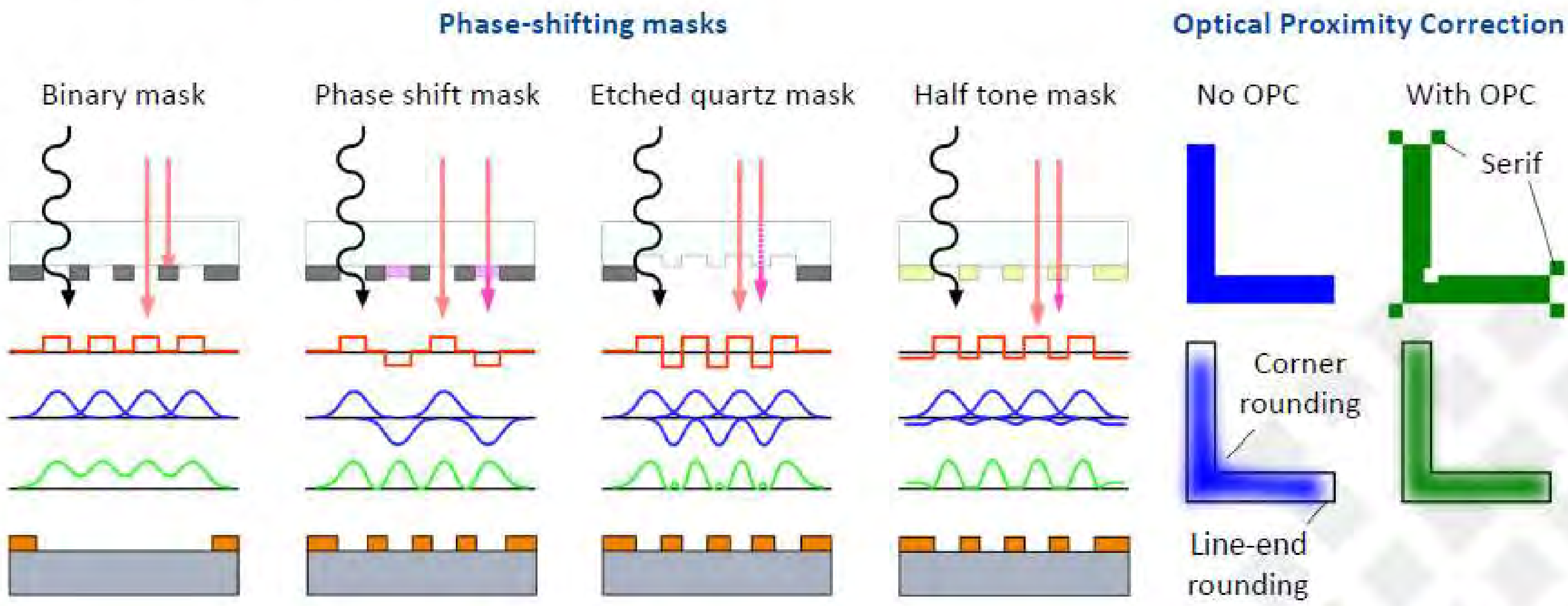




→ The latest lithography technology includes high-resolution EUV, a high-volume chip manufacturing tools with a light source wavelength of 13.5 nm.

B) Reduce the κ_1 factor

- It is a collection of everything else that can be done to improve resolution.
  - Improve the photoresist.
  - Use resolution enhancement methods like phase-shifting masks and off-axis illumination.
- The physical limit for κ_1 is 0.25.



Pushing k_1 further

$$\underset{\text{Half-Pitch}}{CD} = k_1 \left(\frac{\lambda}{NA} \right)$$

Controlling light | **Get pupils into shape** | **Simulating the best blueprint**

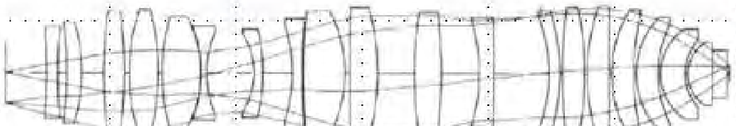
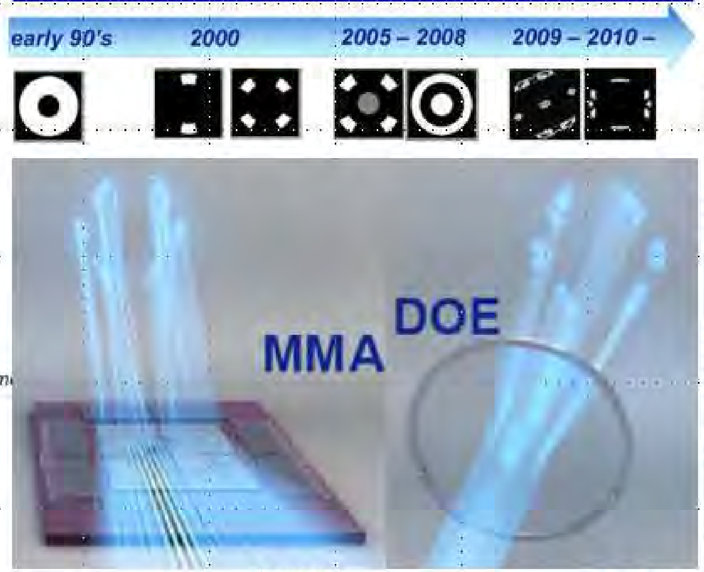
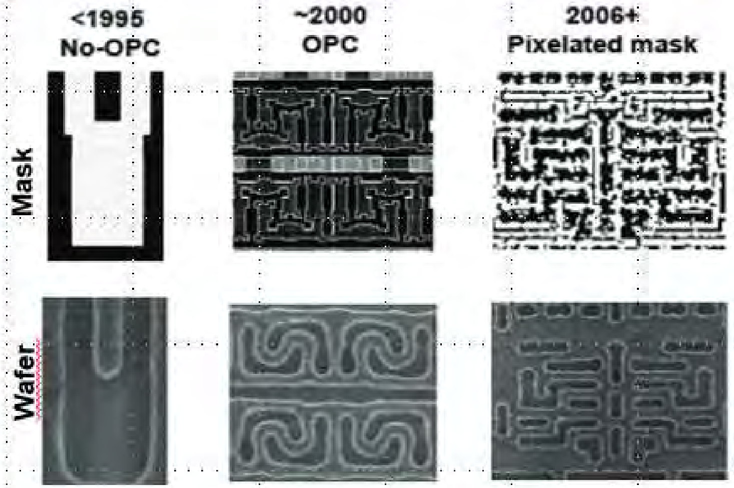
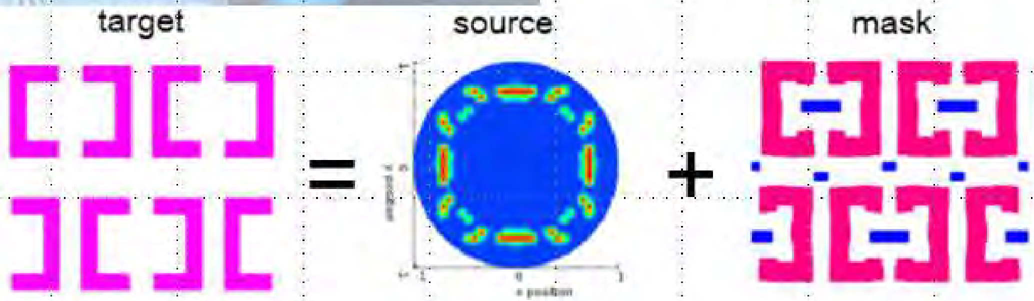


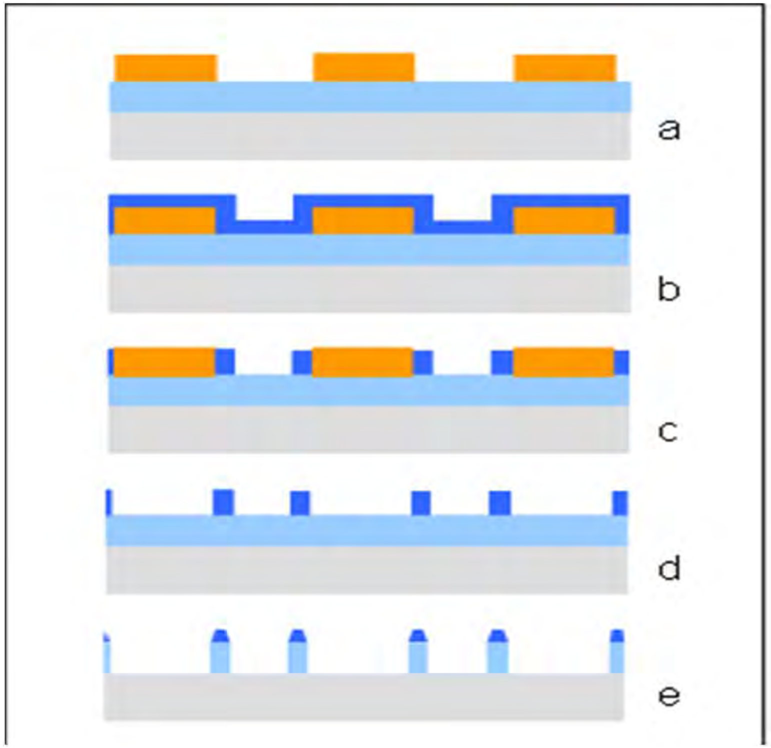
Figure 3.3 Example of a simple NA = 0.8, 248-nm lens design[1]



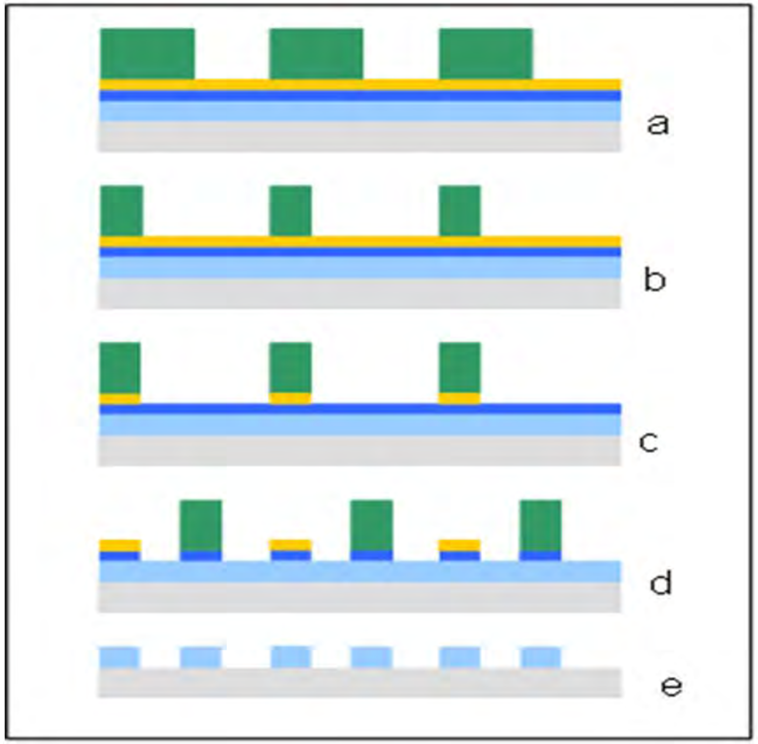




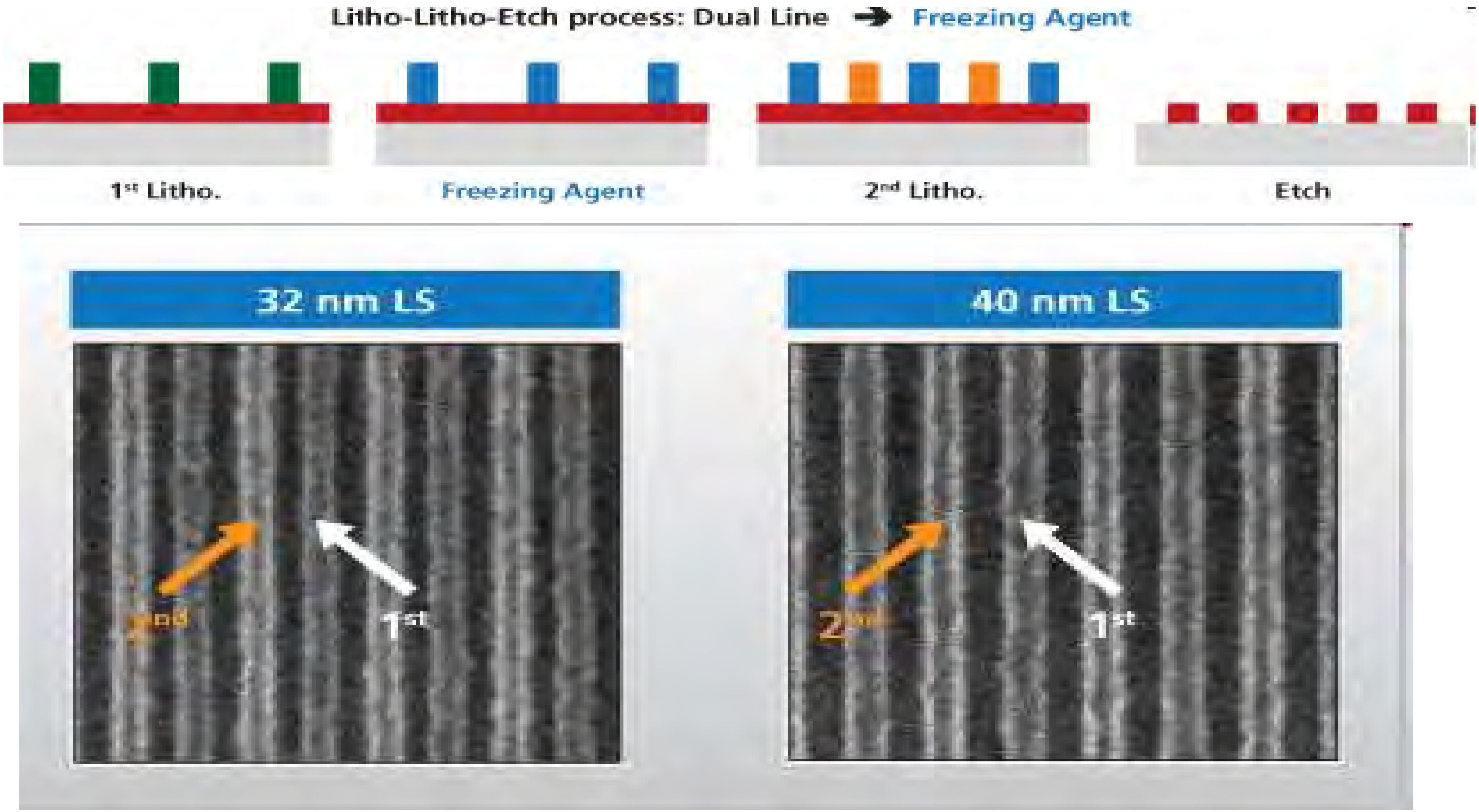
Double patterning techniques



Pitch doubling



Double exposure


Litho-Litho-Etch process: Dual Line → Freezing Agent
1st Litho.
Freezing Agent
2nd Litho.
Etch
32 nm LS
40 nm LS
2nd
1st
2nd
1st

State of the art optical lithography

EUV optical lithography (λ=13.5 nm)

TWINSCAN NXE:3400C (ASML)

EUV volume production at the 7 and 5 nm nodes

170 wafers per hour

Dose: 20mJ/cm2,
Wafer size: 300 mm
Die size: 26 x 33 mm

NA: 0.33
Resolution 13 nm
Overlay accuracy: 1.4 nm

State of the art optical lithography

The latest!

dual-stage EUV optical lithography (λ=13.5 nm, high NA)

TWINSCAN EXE:5200B (ASML)

sub-2 nm Logic nodes and leading-edge DRAM nodes.

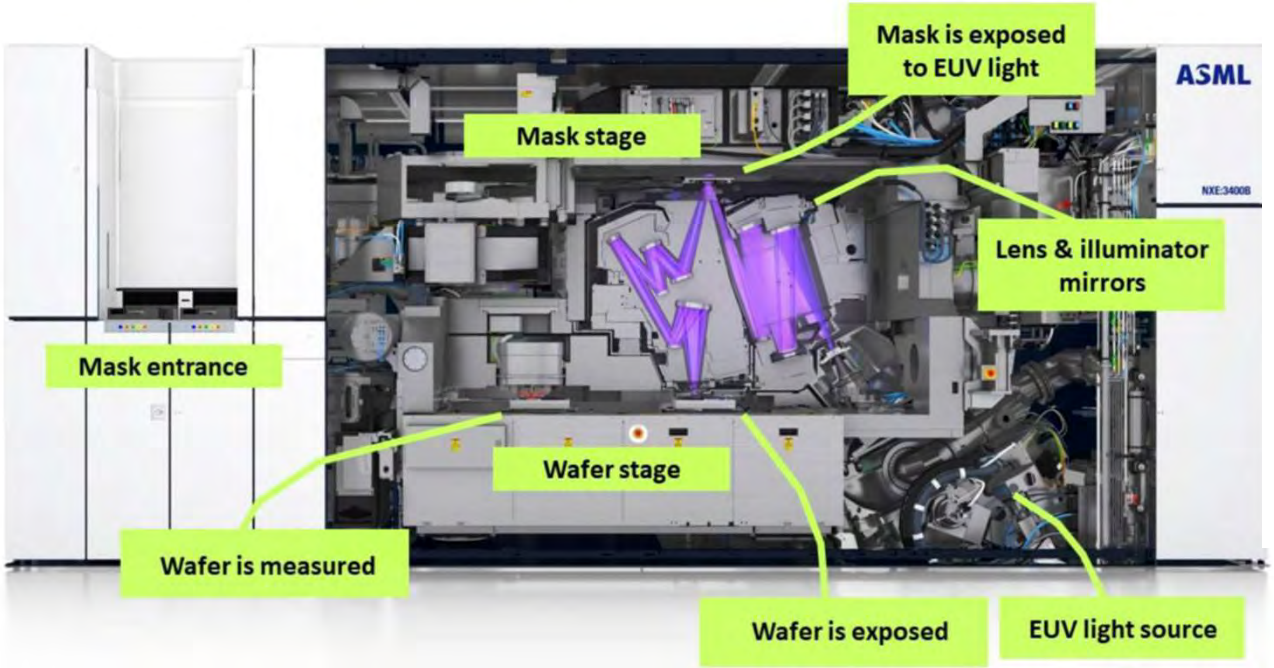
>170 wafers per hour

Dose: 20mJ/cm2,
Wafer size: 300 mm
Die size: 26 x 16.5 mm

NA: 0.55
Resolution 8 nm
Overlay accuracy: 0.6 nm

State of the art optical lithography

EUV optical lithography (λ=13.5 nm)



TWINSCAN NXE:3400C (ASML)

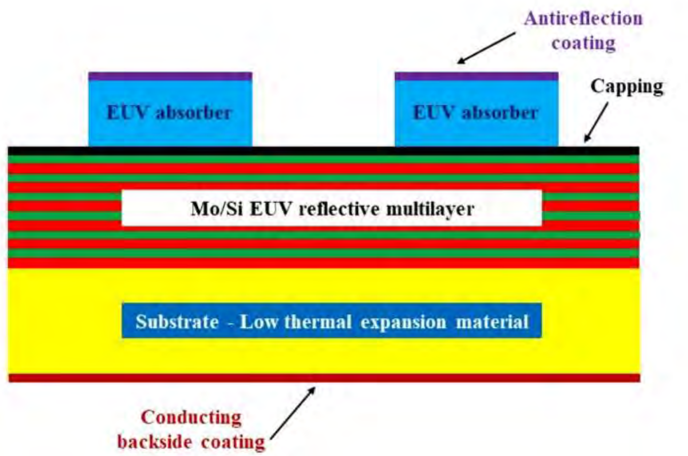
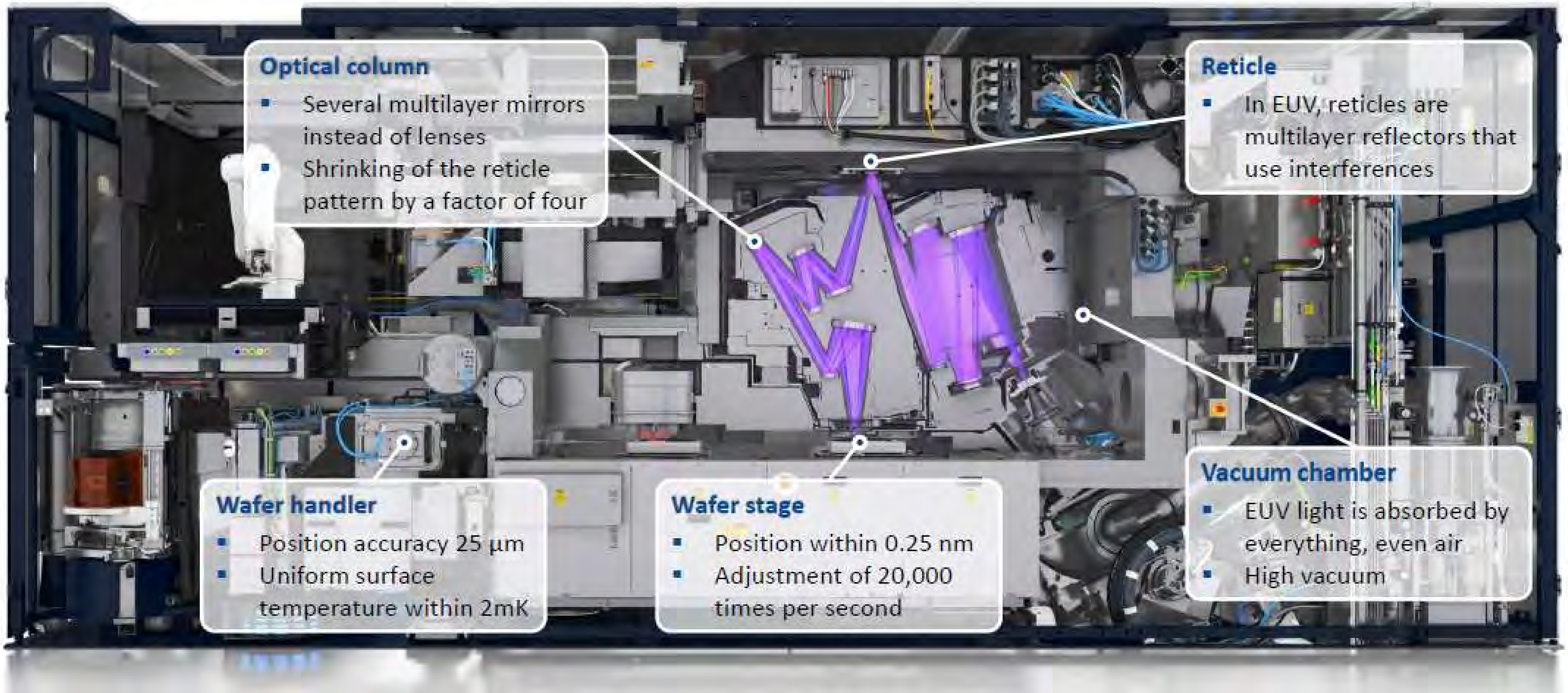
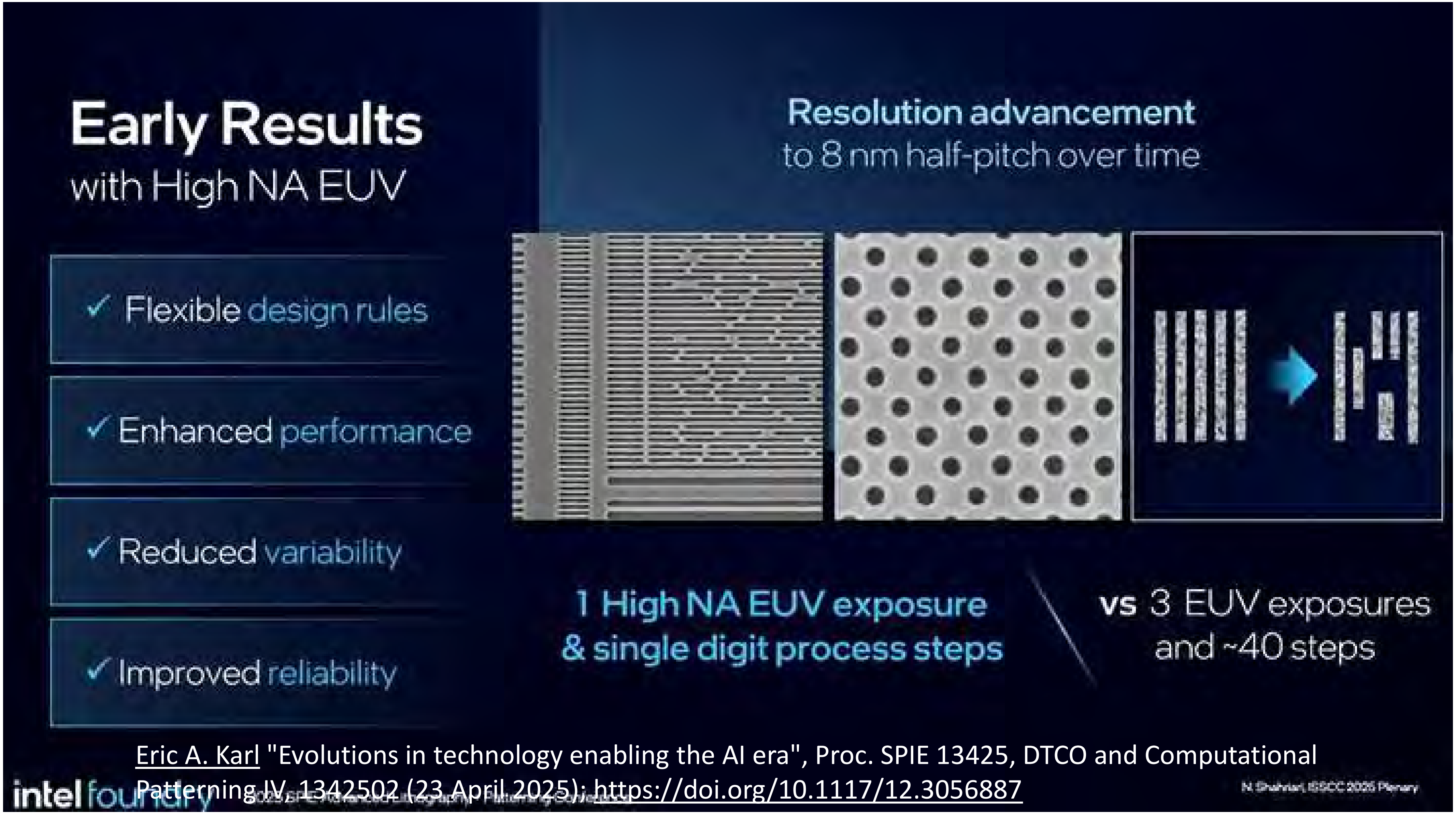


Figure 2.11. Sketch of the cross section of the structure of a EUV lithography photomask.

EUV volume production at the 7 and 5 nm nodes


Optical column
Several multilayer mirrors instead of lenses
Shrinking of the reticle pattern by a factor of four
Reticle
In EUV, reticles are multilayer reflectors that use interferences
Wafer handler
Position accuracy 25 µm
Uniform surface temperature within 2mK
Wafer stage
Position within 0.25 nm
Adjustment of 20,000 times per second
Vacuum chamber
EUV light is absorbed by everything, even air
High vacuum



Eric A. Karl "Evolutions in technology enabling the AI era", Proc. SPIE 13425, DTCO and Computational Patterning IV, 1342502 (23 April 2025); https://doi.org/10.1117/12.3056887

Lithography evolution

- The lithography is the driving force behind the advancement of technology nodes, the technology enabler
- It accounts for 25-35% of the manufacturing costs
- The advancement of lithography resolution was initially achieved through the continous decrease of the exposure wavelength or by increasing the NA

“EUV optics: status, outlook and future”, Paul Graeupner et al, Proceedings Volume 12051, Optical and EUV Nanolithography XXXV; 1205102 (2022)
https://doi.org/10.1117/12.2614778

Table LITH-2 Potential Solutions for Leading-Edge Logic Lithography

	2022	2025	2028	2031	2034	2037
Logic node	3 nm	2.1 nm	1.5 nm	1.0 nm	0.7 nm	0.5 nm
Node	G48M24	G45M20	G42M16	G40M16T2	G38M16T4	G38M16T6
Minimum ½-pitch	12 nm	10	8 nm	8 nm	8 nm	8 nm
Primary options for logic	EUV 0.33.NA multiple patterning	EUV 0.33.NA multiple patterning EUV 0.55.NA single patterning	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)
Potential solutions for cost reduction, LER reduction		Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA

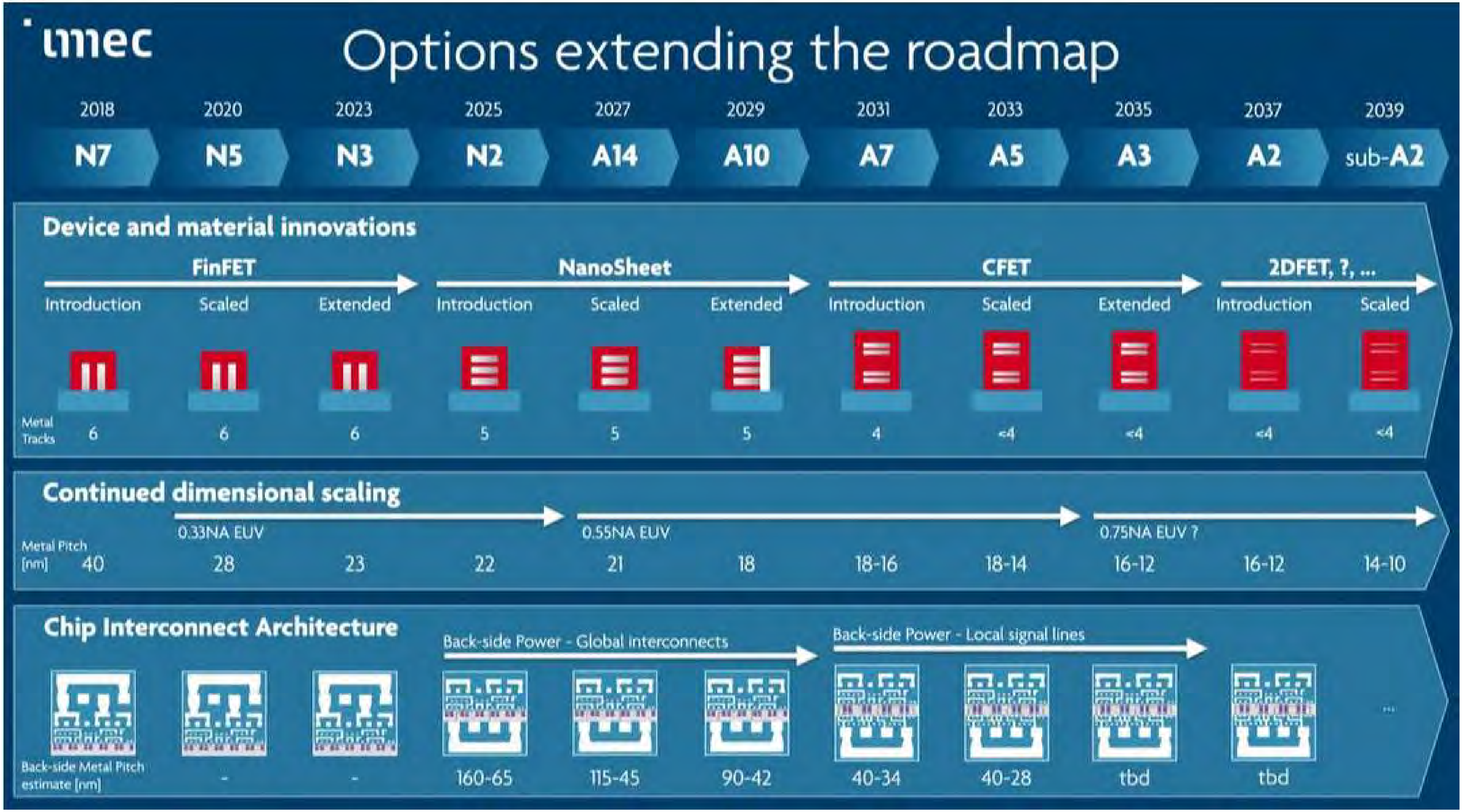
INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

FUTURE TRENDS:

IEEE IRDS ROADMAP

The IRDS™ is a set of predictions that intent to provide a clear outline to simplify academic, manufacturing, supply, and research coordination regarding the development of electronic devices and systems.

"The endless progression of Moore's Law", Luc Van den hove, Proceedings. Volume PC12053, Metrology, Inspection, and Process Control XXXVI; PC1205301 (2022)



Christophe Fouquet. ASML. **Scaling to support Moore's Law through the AI era**. SPIE Advanced Lithography and Patterning. San Jose, CA. 2025

Take home messages

Optical lithography is the most used lithography method because of its robustness, reliability and throughput

Optical lithography uses UV optical radiation to expose a photosensitive resist

Resolution in optical lithography is limited by diffraction

There are three modes of mask based optical lithography: contact, proximity and projection

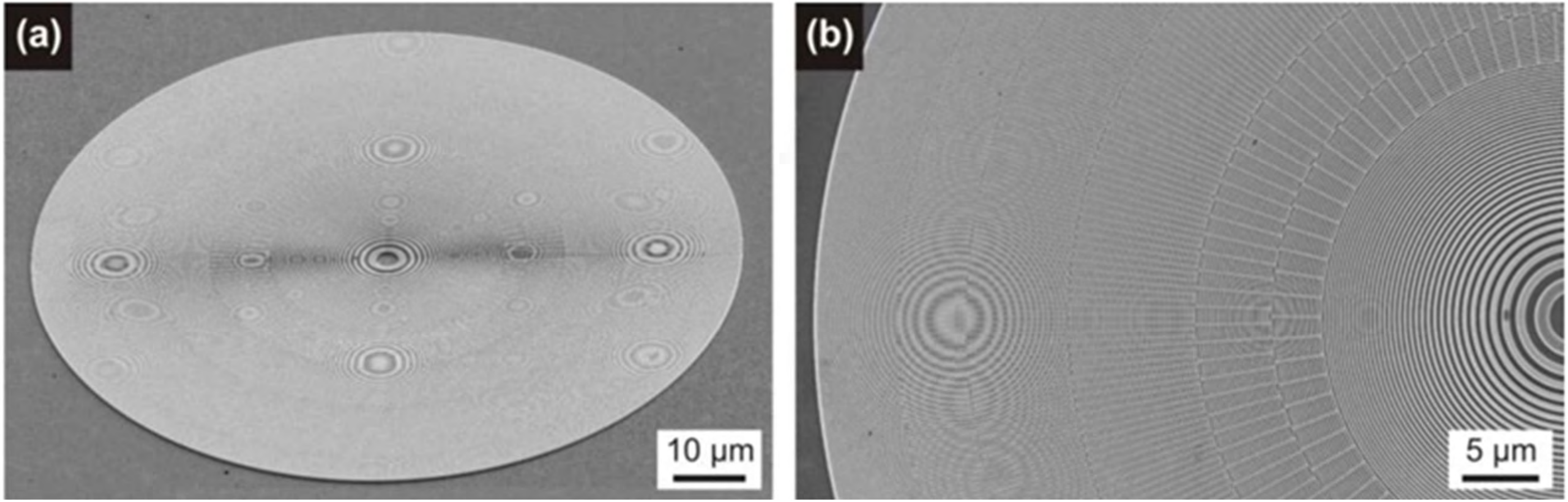
The achievable resolution depends on the wavelength and the optical lithography mode

Tricks to improve the resolution include: reducing wavelength, increasing numerical aperture (immersion lithography, múltiple patterning, optical proximity correction and phase-shift masks)

State of the art optical lithography uses EUV radiation and complex and expensive equipment

Other forms of optical lithography are **laser lithography, interference lithography and 2-photon polarization**

Electron beam lithography



Joan Vila-Comamala, Sergey Gorelick, Elina Färm, Cameron M. Kewish, Ana Diaz, Ray Barrett, Vitaliy A. Guzenko, Mikko Ritala, Christian David, "Ultra-high resolution zone-doubled diffractive X-ray optics for the multi-keV regime," Opt. Express **19,** 175-184 (2010); https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-1-175

Question:

- What it limits resolution in optical lithography?

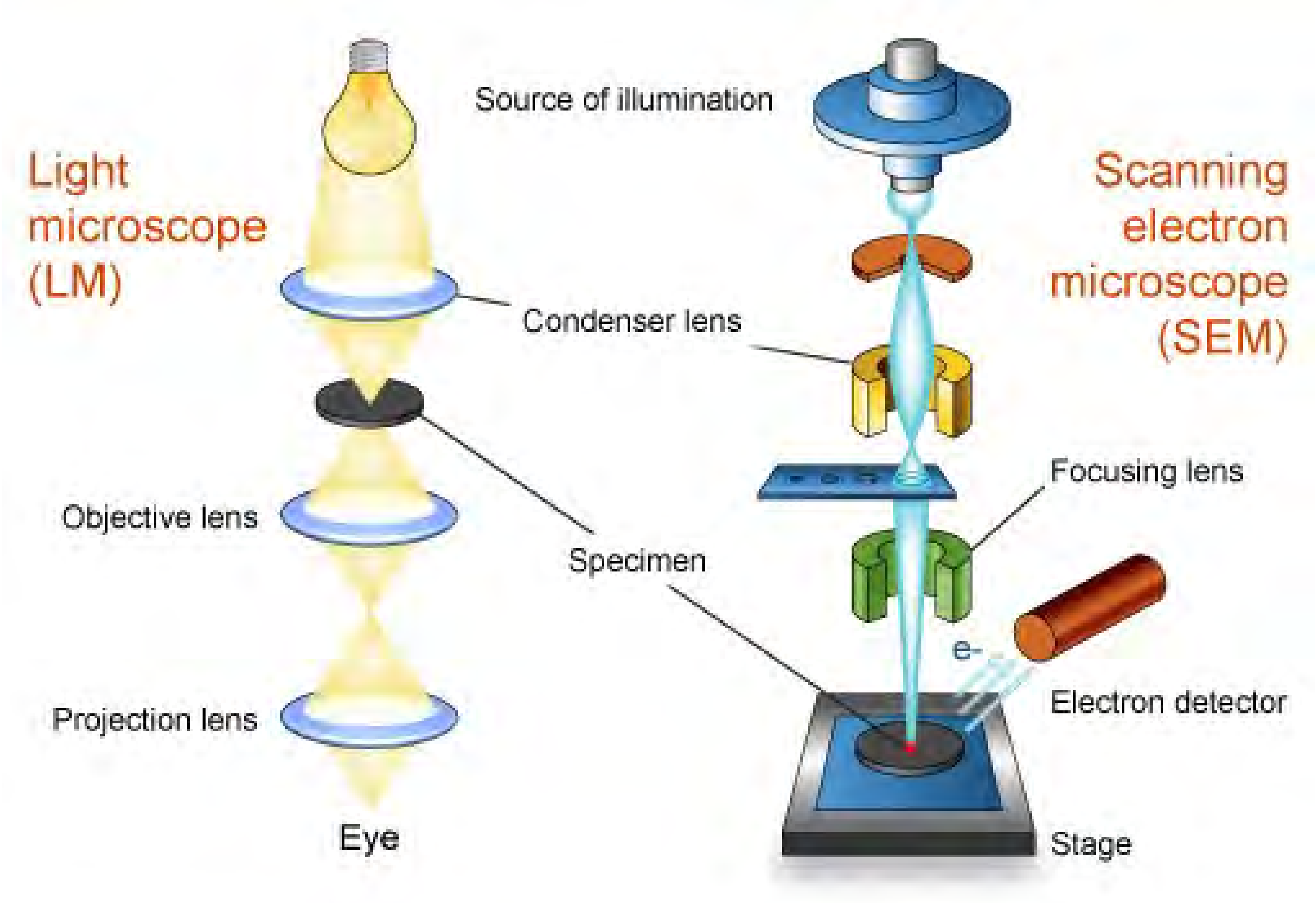
- In optical lithography, diffraction phenomena limits the resolution
- Reducing the wavelength of the optical radiation has been one of the ways to improve the resolution

Resolution in projection optical lithography

$$R = k_1 \frac{\lambda}{NA}$$

Electrons wavelength: $\lambda_e = \frac{1.226}{\sqrt{V}}$ (nm) <0,1Å!!

Optical vs Electron beam lithography

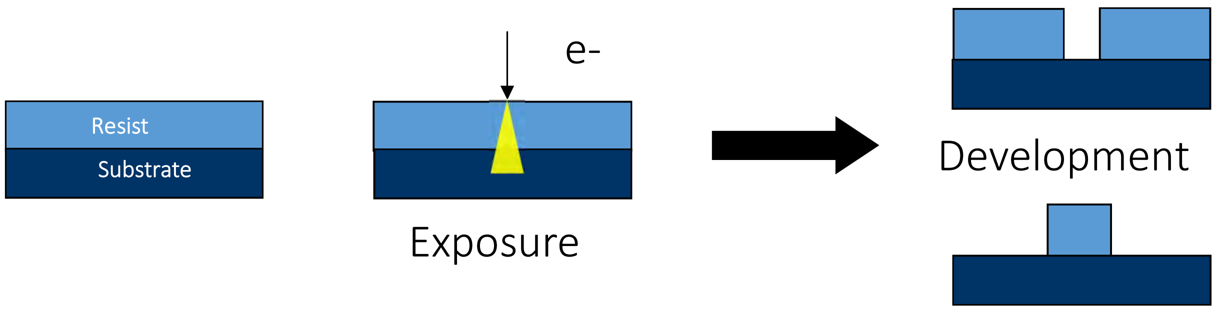


Electron beam lithography is the most commonly used nanolithography method in research

Electron beam lithography (EBL)

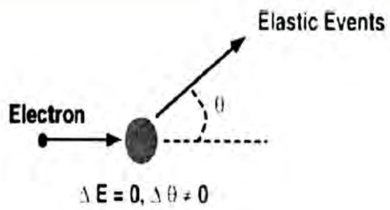
Concept

- Exposure of a focused electron beam on a electron sensitive layer of material (EBL Resist)
- Upon exposure, chemical/physical properties of the resist change
- After development, areas of the resist are selectively eliminated

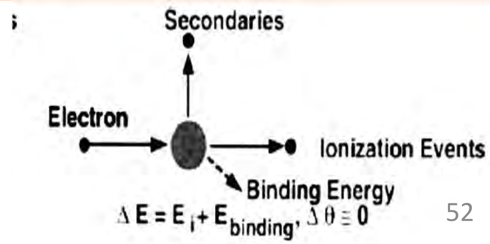


Resolution in electron beam lithography is limited by the scattering of electrons with the atoms of the resist and substrate

Elastic scattering

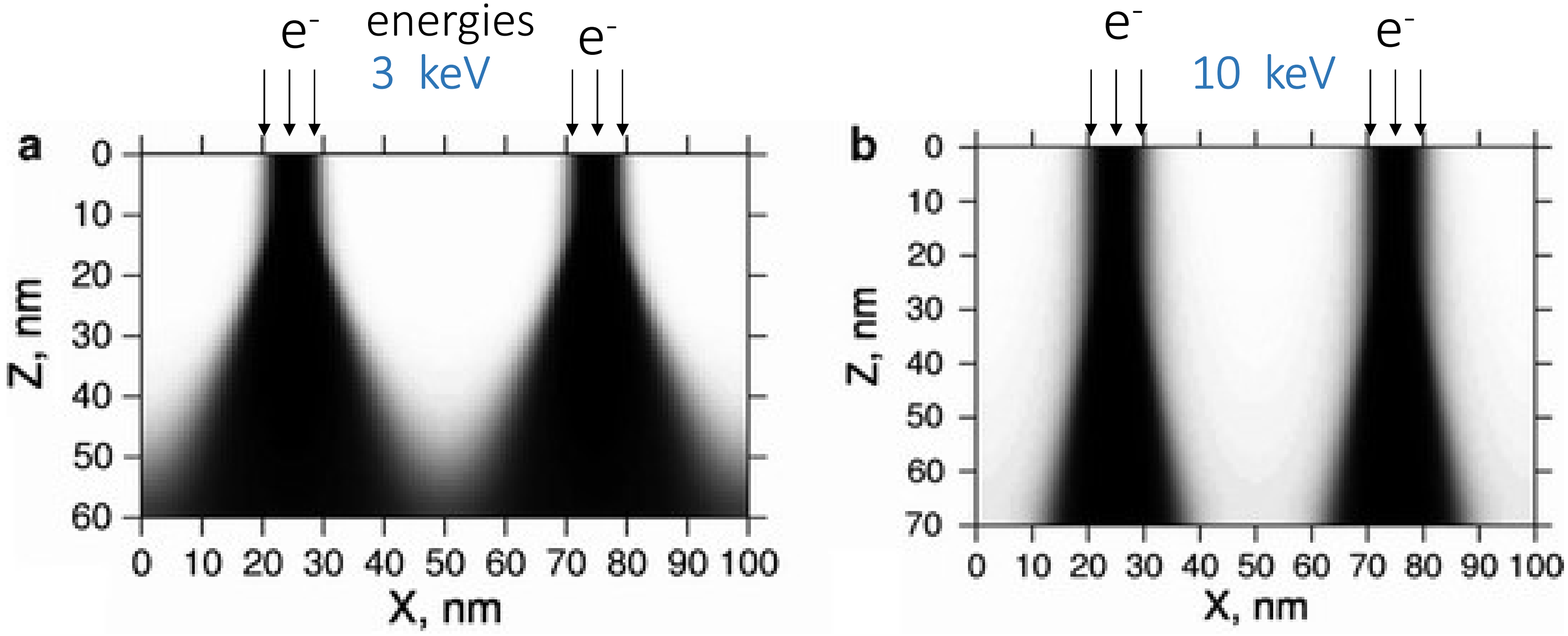


Inelastic scattering



Forward scattering

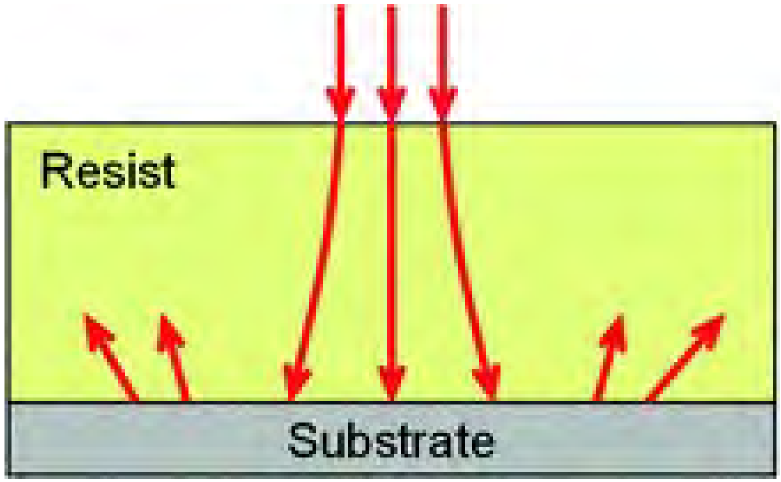
As the electrons enter the resist, they begin a series of low energy elastic collisions, each of which will deflect the electron slightly. This forward scattering broadens the beam by an amount that increases with thickness, and this effect is more pronounced at low incident energies



Mohammad M.A., Muhammad M., Dew S.K., Stepanova M. (2012) Fundamentals of Electron Beam Exposure and Development. In: Stepanova M., Dew S. (eds) Nanofabrication.

Backscattering

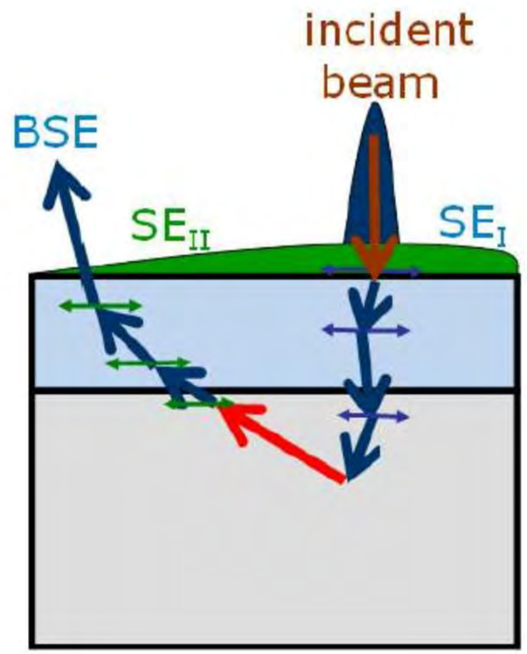
Most of the electrons pass entirely through the resist and penetrate deeply into the substrate. Some fraction of those electrons will eventually undergo enough large angle collisions to re-emerge into the resist at some distance from the point at which they left it. At higher energies, these backscattered electrons may cause exposure microns away from where the beam entered. This leads to the so-called proximity effect



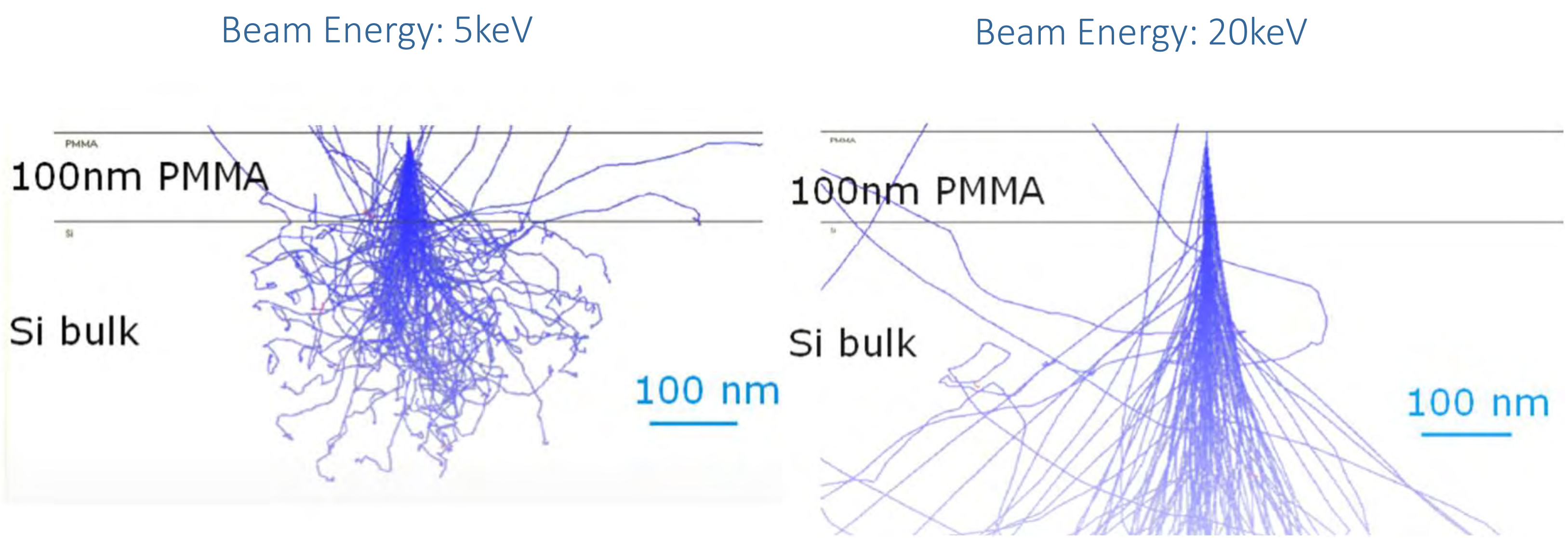
Mohammad M.A., Muhammad M., Dew S.K., Stepanova M. (2012) Fundamentals of Electron Beam Exposure and Development. In: Stepanova M., Dew S. (eds) Nanofabrication.

Secondary electrons

Secondary electrons are low energy (10-100 eV) produced by inelastic collisions of the incident electrons. They have short travelling range and fix a limits for the minimum resolution .



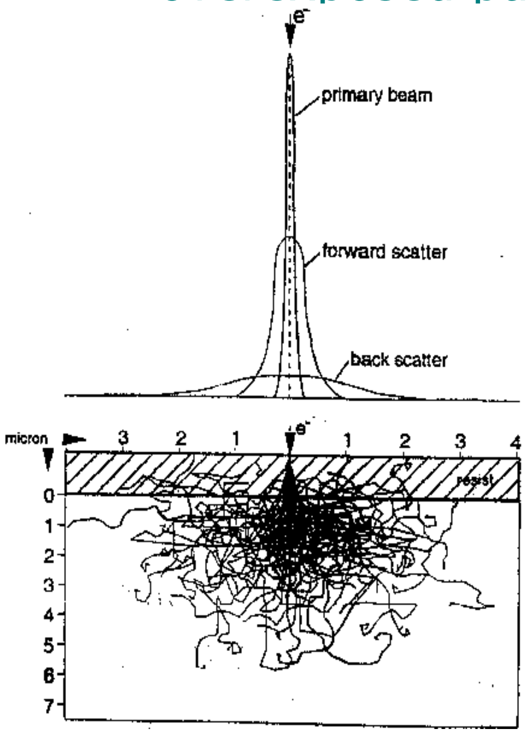
Monte Carlo simulations

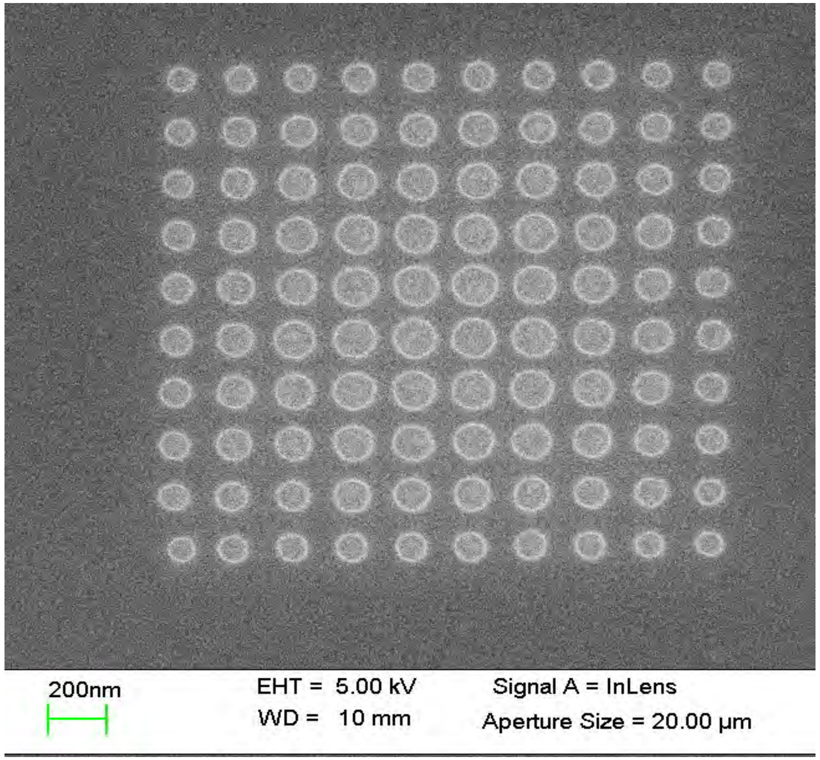


Trajectory of the incident electrons. Each change of direction causes the emission of a secondary electron

Exposure Process: Proximity Effect

Due to backscattered electrons the resist is also exposed in nearby areas. When exposing a dense pattern this leads to overexposed patters



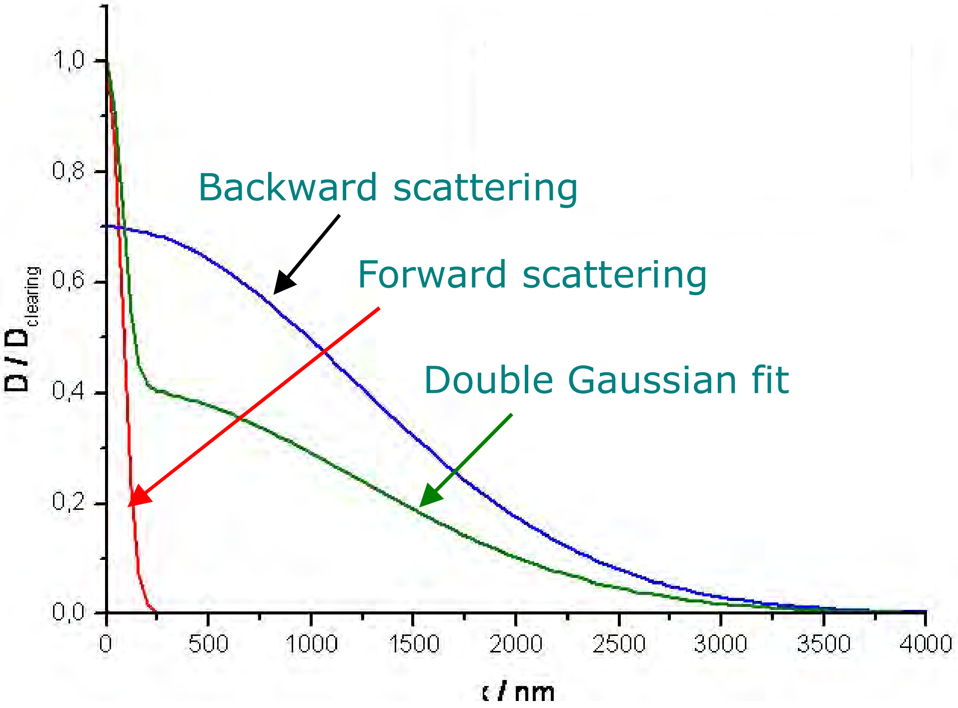


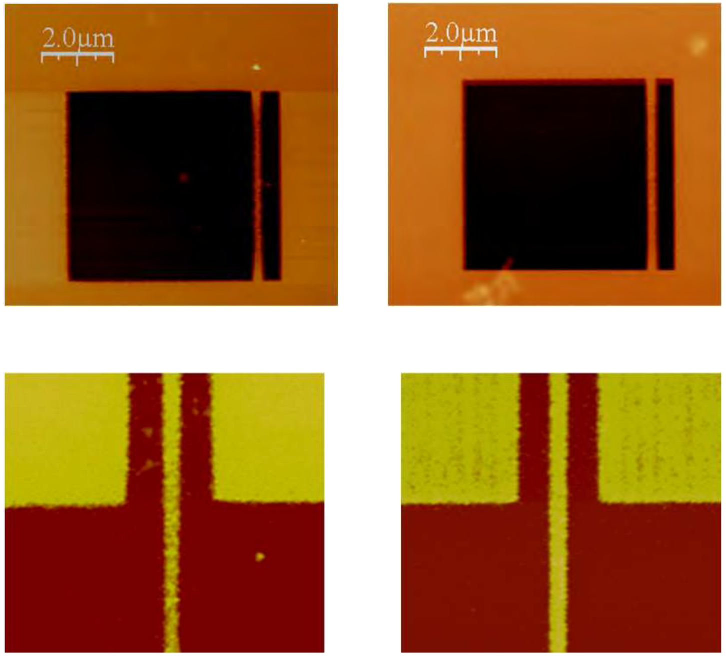
- In the borders of dense or continous patterns
- Mixing small and big features

Proximity Effect Correction: modelling and dose re-calculation

$$f(r) = \frac{1}{\pi(1+\eta)}\left(\frac{1}{\alpha^2}\exp\left[-\left(\frac{r}{\alpha}\right)^2\right] + \frac{\eta}{\beta^2}\exp\left[-\left(\frac{r}{\beta}\right)^2\right]\right)$$

α = range of forward scattering
β = range of backward scttering
η = ratio of energy deposited by forward scatterd electrons to the energy deposited by backscattered electrons

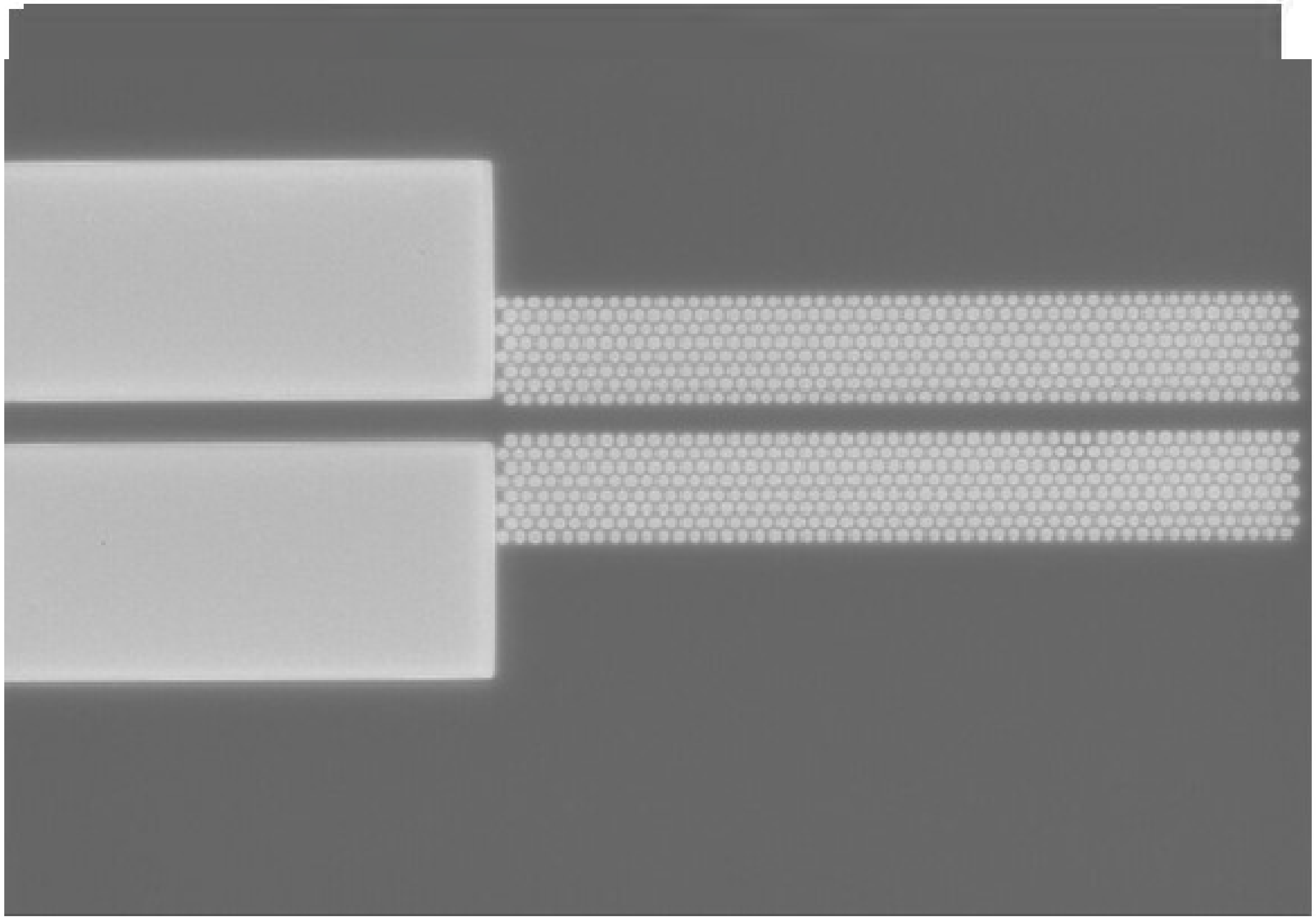




PMMA		α	β	η
10 keV	(µm)	0.4	0.6	0.75

mr–EBL 6000.1		α	β	η
10 keV	(µm)	0.3	0.6	0.75

Proximity effect correction: example



Throughput

Estimation of exposure time in electron beam lithography

Situation	Resist sensitivity ($\mu C/cm^2$)	Beam current (pA)	Area to pattern (μm^2)	Time (h) (1s=0.0003h)	Thorughput ($\mu m^2/h$)	
Typical (PMMA)	**200**	**100**	**1**	**0.02**	**50**	
High sensitiviy resist (PBS)	1	100	1	0.0001	10,000	
Low beam current	200	1	1	2	0.5	
Large area	200	100	100	2	50	*0.001 m^2/h*
Fast limit	1	10,000	100	0.0001	1,000,000	
Slow limit	200	1	100	200	0.5	

(*) Rough estimation without taking into account proximity effect corrections, design issues, patterning strategies, beam displacement, settle time

Resolution limits

<u>Beam resolution</u>

Thick resists (forward scattering)

Thin resists (secondary electrons, back scattering)

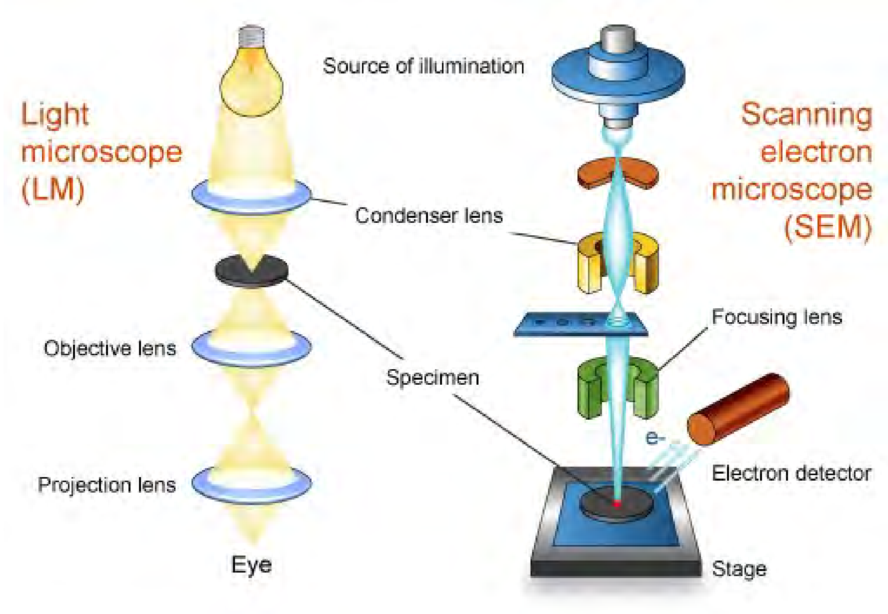
Secondary electron range (~5-10nm)

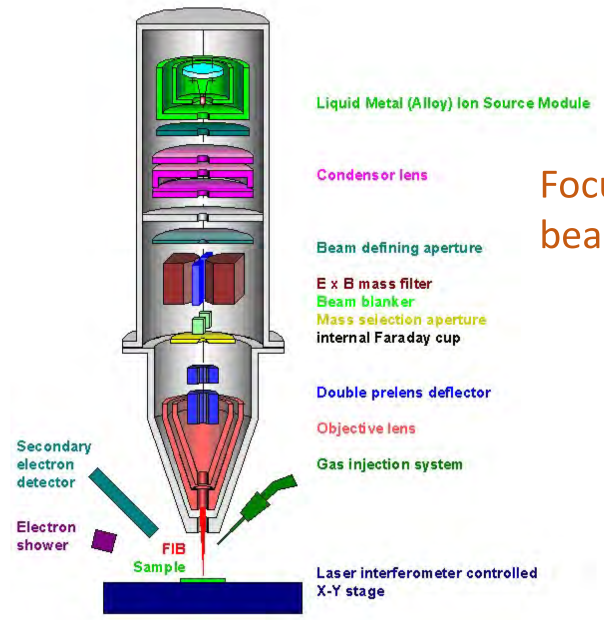
<u>Resist limits</u>

- Polymer size (~5-10nm)
- Chemically amplified resists (acid diffusion ~50nm)

<u>In practice, the achievable resolution in polymeric resists is around 10-20nm</u>

Focused Ion Beam (FIB) fabrication



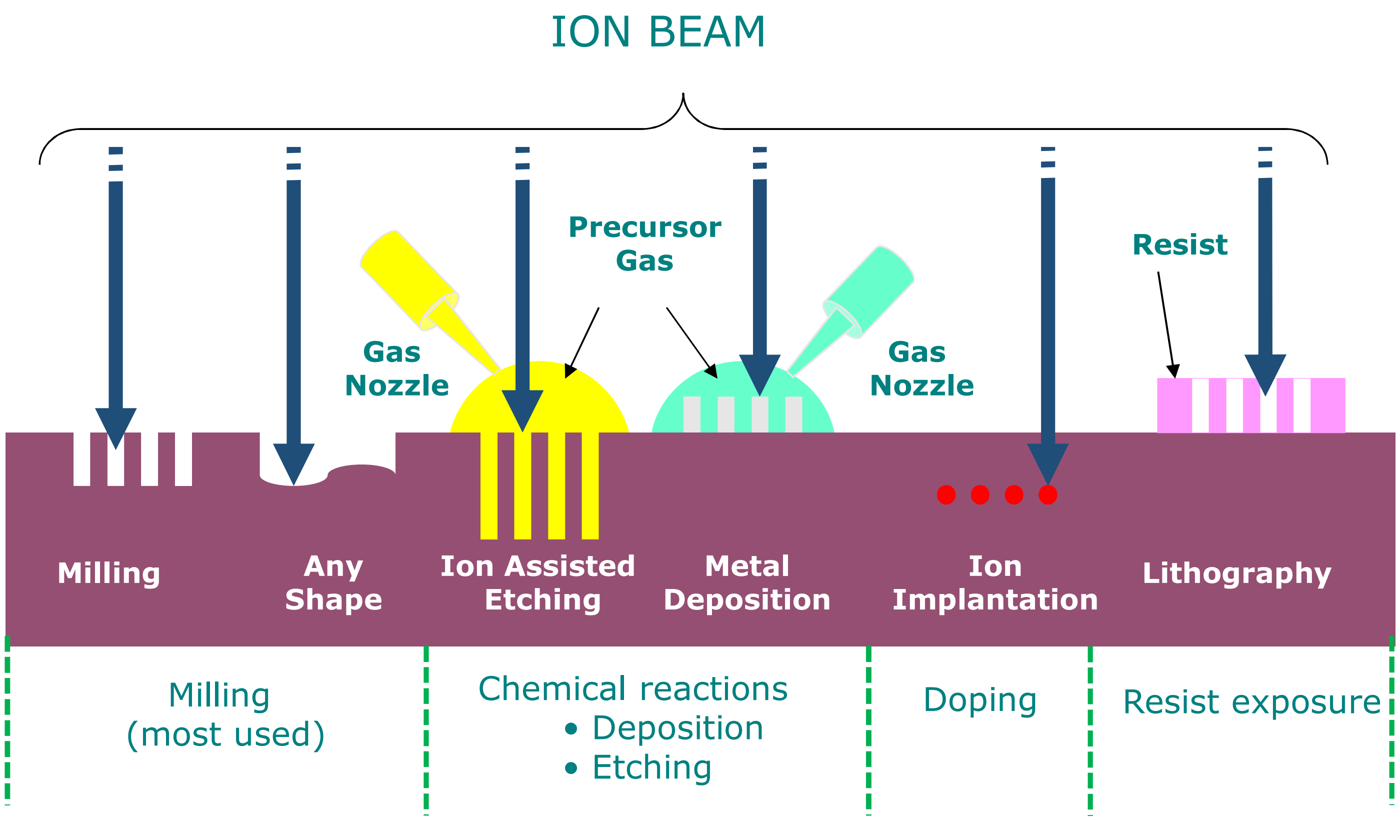


Focused ion beam system

Concept:

- Exposure of a surface by a focused ion beam
- Multiple modes of operation: Resist exposure (lithography), direct writing (milling), induce reactions, doping, …
- Ions have much large mass than electrons

Ion beam interaction processes with surfaces

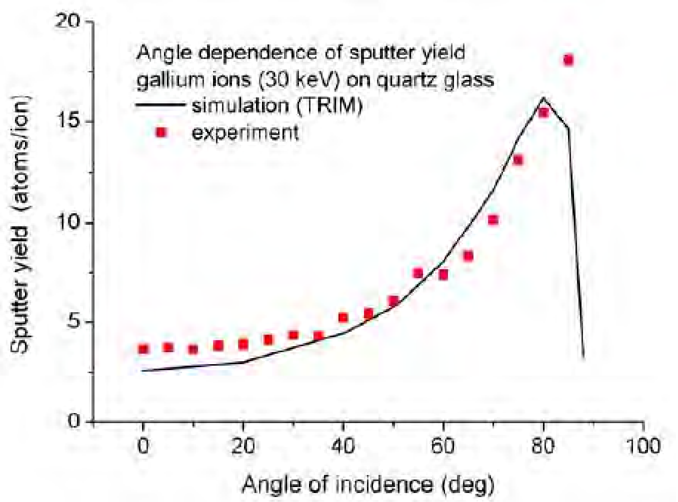


Milling

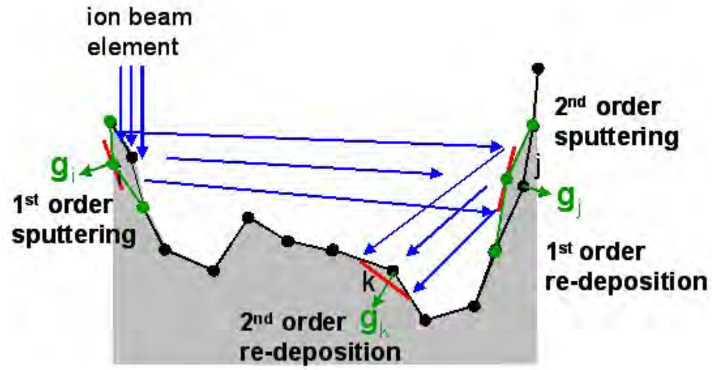
Milling is a process combining physical sputtering, material re-deposition, and amorphization (swelling)

Sputtering: An atom from a material in the solid phase is ejected into the gas phase. It is the major mechanism for material removal

30kV Ga+	Sputtering yield (atoms/ion)	Sputtering Rate (cm^3/nC)
Si	2.1	0.27
Al	2.9	0.3
Au	25	1.5



Re-deposition: the sputtered atoms tend to condense back into the solid phase upon collision with any solid surface nearby and a portion of the ejected atoms may bump into the already sputtered surface and redeposit on it.



Redeposition can be greatly reduced if multiple passes instead of a single pass are used in milling with the same amount of ions. With multiple passes, each successive pass removes redeposited material from the previous pass.

Redeposition reduces the milling rate and the aspect ratio of the milled structures

Milling

Milling is a process combining physical sputtering, material re-deposition, and amorphization (swelling)

Amorphization: If the energy or dose level of the incident ions is not high enough for sputtering, amorphization may occur in the bombarded area of a crystalline substrate and may induce the substrate to swell.

In the case of a crystallized Si substrate bombarded by Ga ions, the dose level that causes amorphization is on the order of 10^{15} ions·cm^{-2}, while the effective sputtering dose is more than two orders of magnitude higher

The incident ions in most cases are buried in the target material and may also displace the target atom: Implantation and swelling

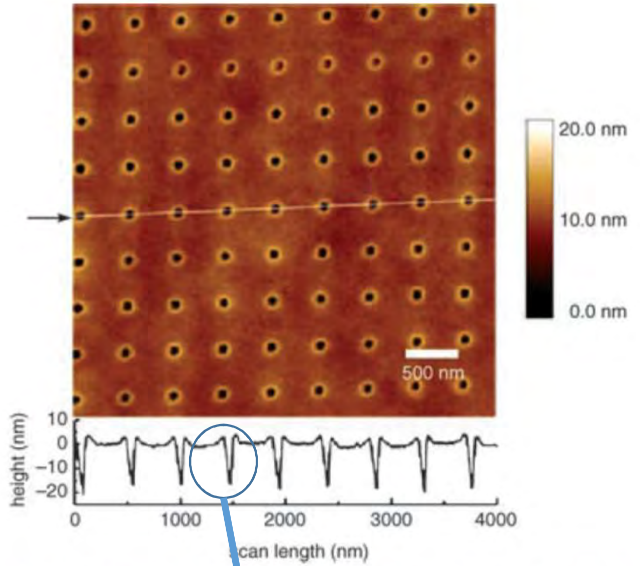
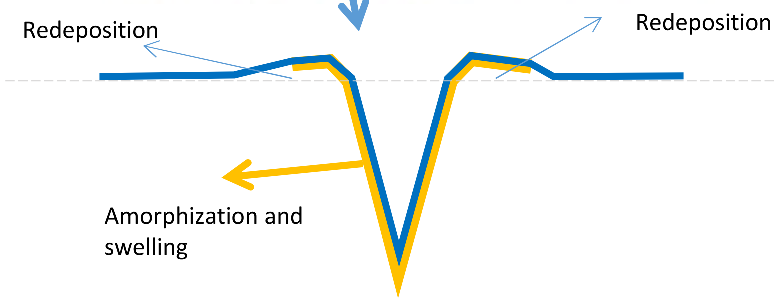


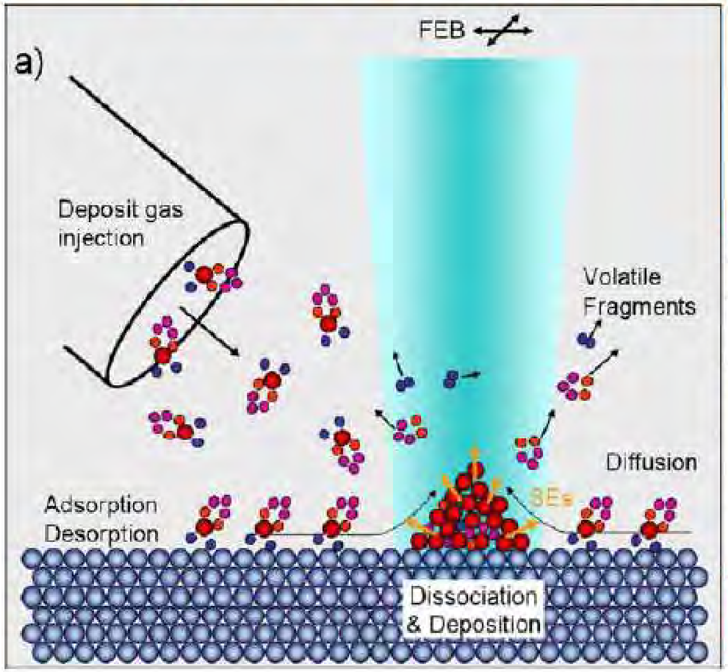
Figure 1. AFM image of hole (dot) array milled by a 30 keV Ga+ FIB at 1 pA on a Si substrate (after Li et al.[13]).

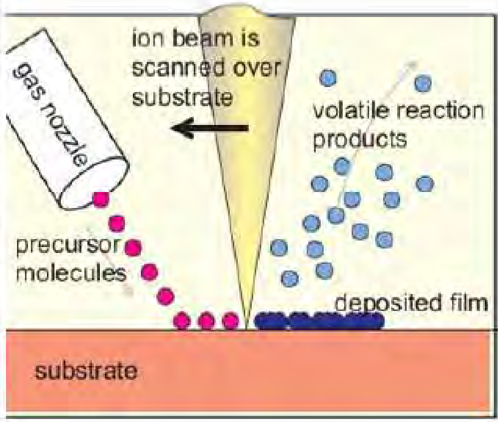


Focused ion beam induced deposition (FIBID)

Decomposition of the gas by the ion beam

- Deposition of the non-volatile components on the



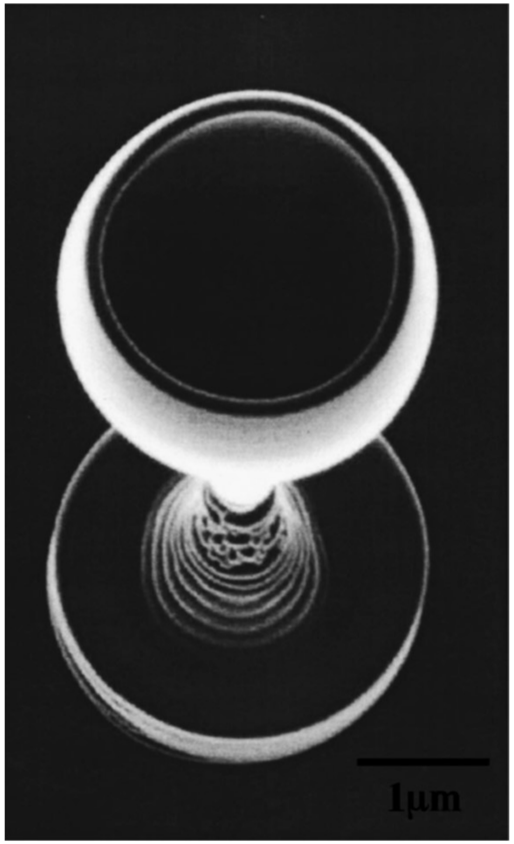


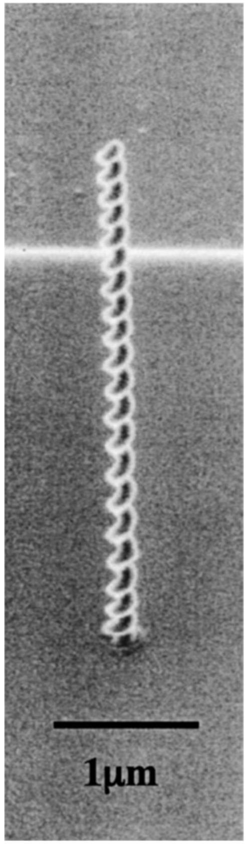
Gas	Ion, Energy	"Yield" (atoms/ion)	Deposit Composition	Resistivity ($\Omega \cdot$ cm)
WF_6	Ar^+, 500 eV and 2 keV		W:F:C 93.3:4.4:2.3	15
$W(CO)_6$	Ga^+, 25 keV	2	W:C:Ga:O 75:10:10.5	150–225
$C_7H_7F_6O_2Au$	Ga^+, 40 keV (room temp.)	3–8	Au:C:Ga 50:35:15	500–1500 (bulk Au = 2.44)
	Ga^+, 40 keV at 120°C	3	Au:C:Ga 80:10:10	3–10
$C_9H_{17}Pt$	Ga^+, 35 keV	0.2–30	Pt:C:Ga:O 45:24:28:3 25:55:19:2	70–700 (Bulk Pt = 10.4)
$(CH_3)_3NA1H_3$	Ga^+, 20 keV	4–6	Al:Ga:C:N	900
Cu(hfac)TMVS	Ga^+, 25–35 keV	10–30	Cu:C 60:50 (25°C) 95:5 (100°C)	100 5
TMOS + O_2	Si, 60 kV	1 mol/ion	SiO_x	2.5×10^6
OMCTS + O_2	Ga, 50 kV		Si:O:Ga 27:56:17	1.2×10^7
TEOS	Ga, 30 kV			10^8
PMCPS	Ga, 30 kV		SiO_x	8×10^{11}

J.Melngailis, U. Maryland

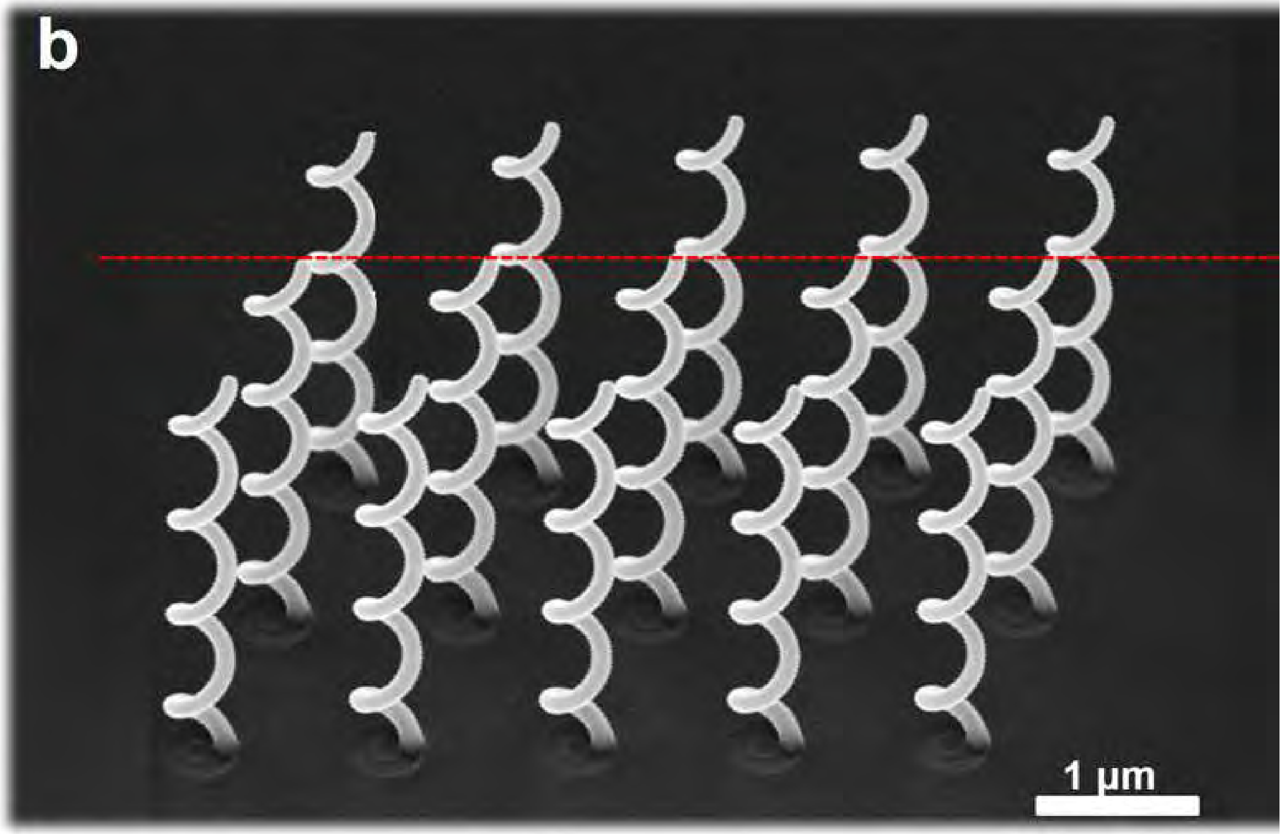
Courtesy of Dr. Albert Romano. UB

Focused ion beam induced deposition (FIBID)





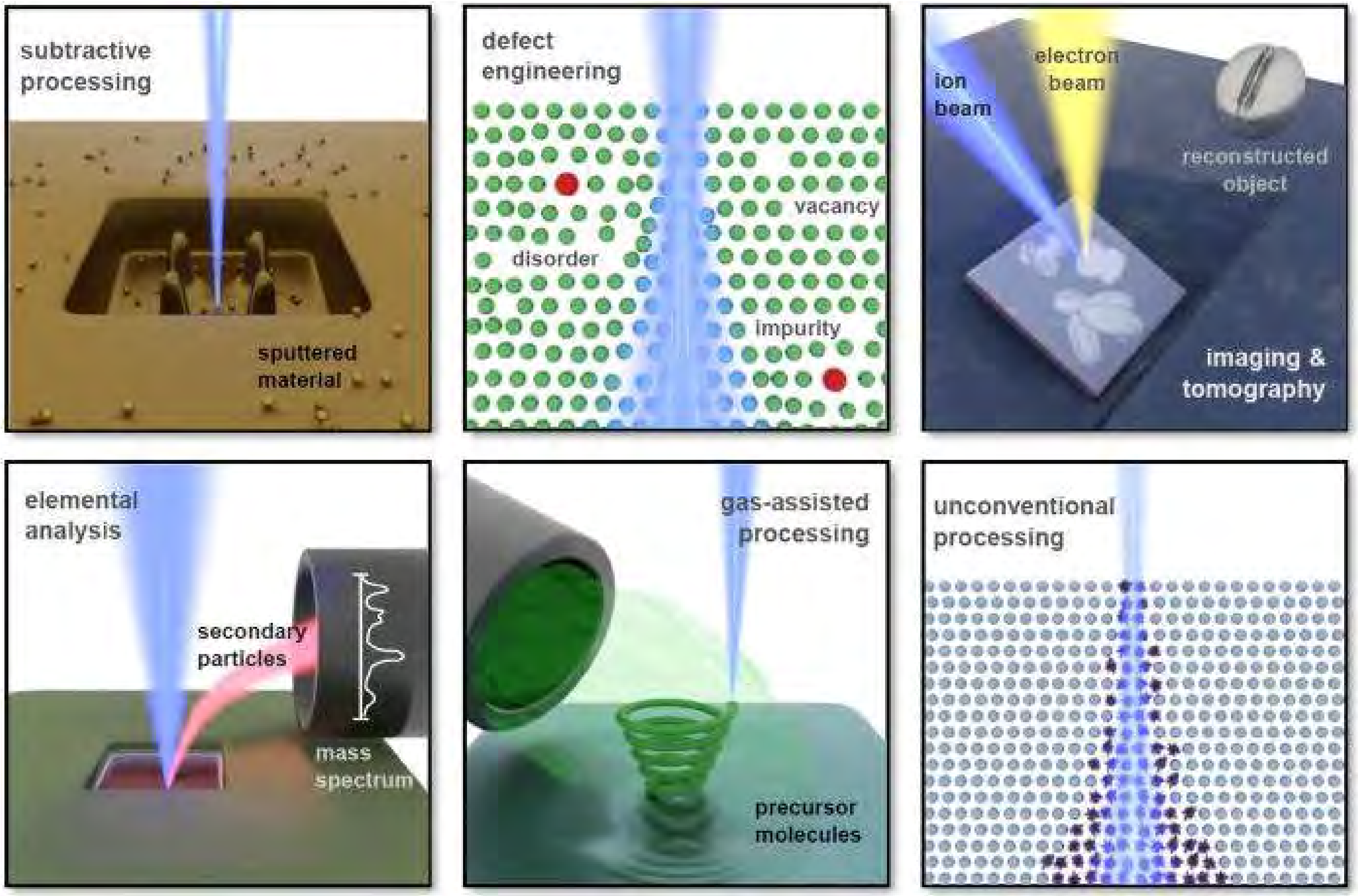
Pt Nanohelices



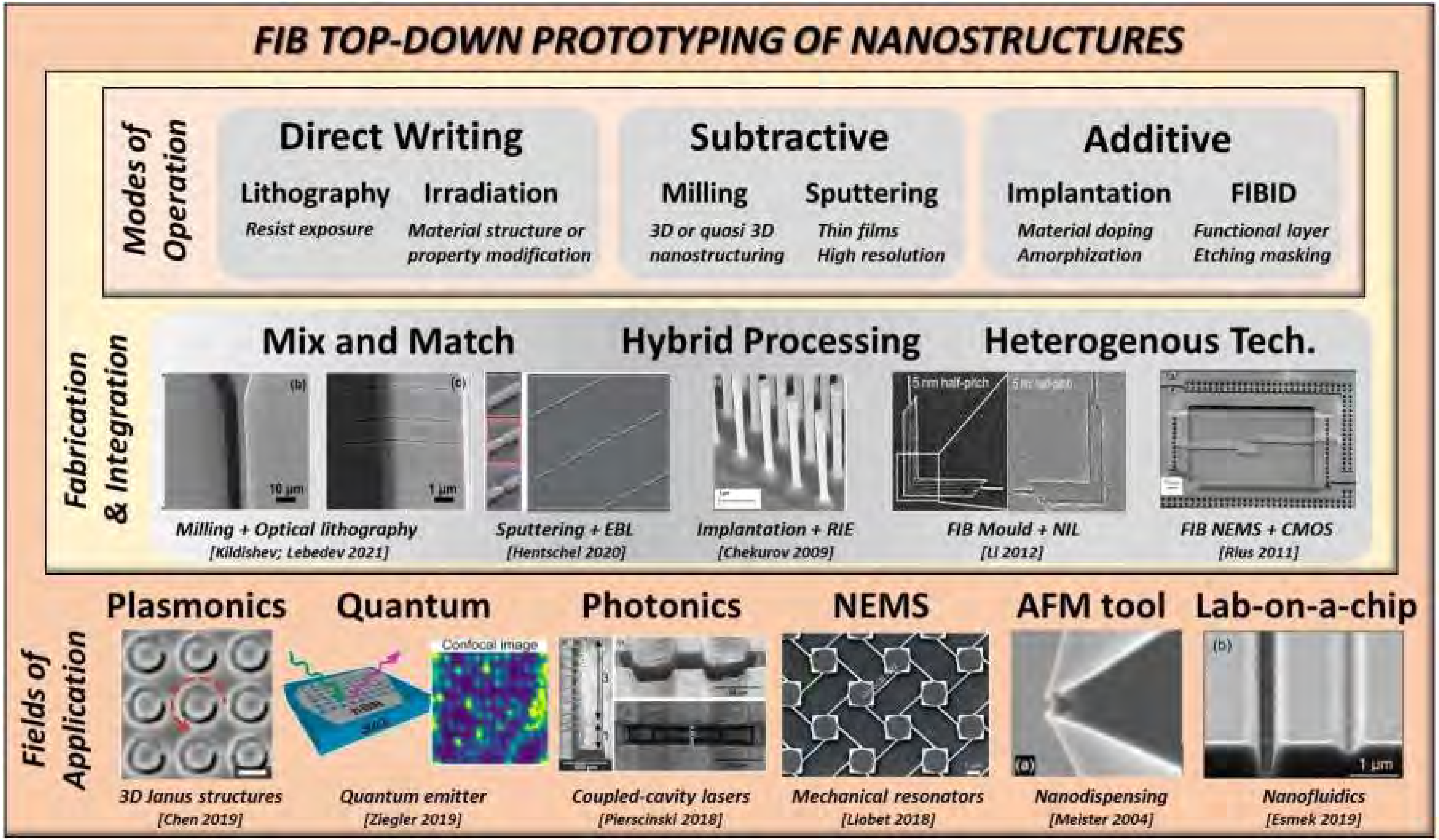
A.A. Tseng Small. 2005

Esposito et al. ACS Photonics. 2015

Focused ion beam techniques

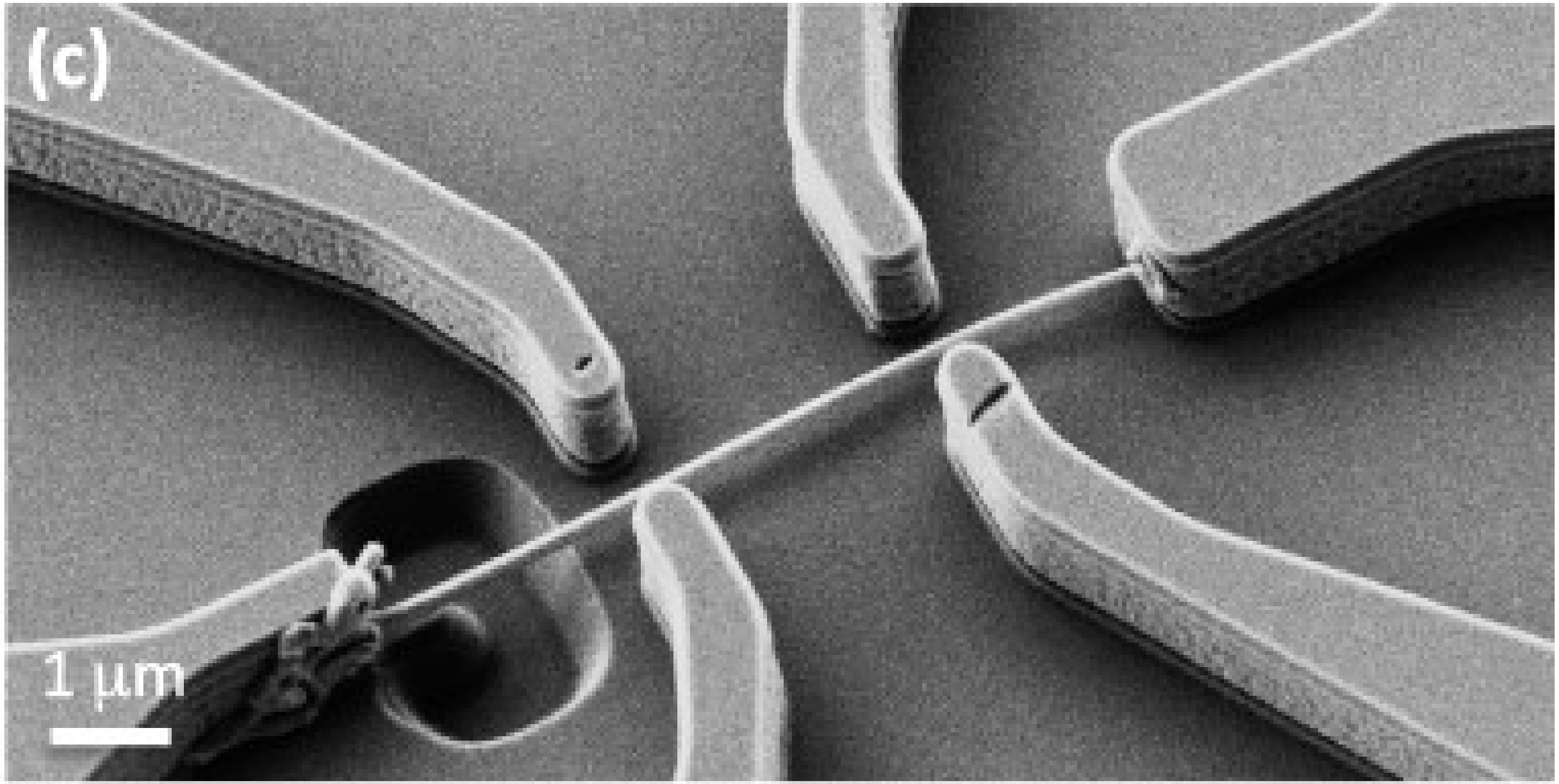


K. Höflich et al. Roadmap for focused ion beam technologies. *Appl. Phys. Rev.* 10, 041311 (2023)



G. Rius, F. Perez-Murano Unpublished

Botom-up fabrication



Fernandez-Regulez et al (2013)

Nanofabrication: Bottom-up vs top-down

Top-down Nanofabrication

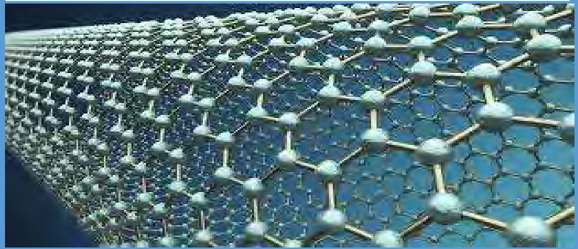
- Resolution limited by resolution
- Surface defects, roughness and crystallographic damage
- No assembly step is needed
- Low defectivity
- Costly

Bottom-up Nanofabrication

- High resolution, limited by the size of the building blocks
- High throughput at low cost
- Device fabrication difficult (position, orientation…)
- Less flexibility
- More defectivity but better pattern fidelity

Examples of bottom-up fabrication

Carbon nanotubes transistors

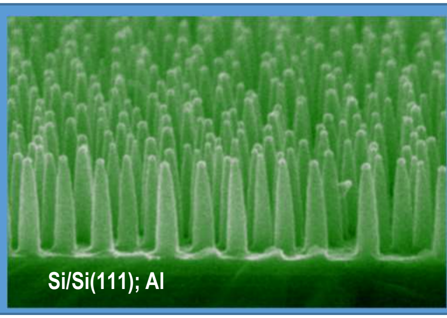


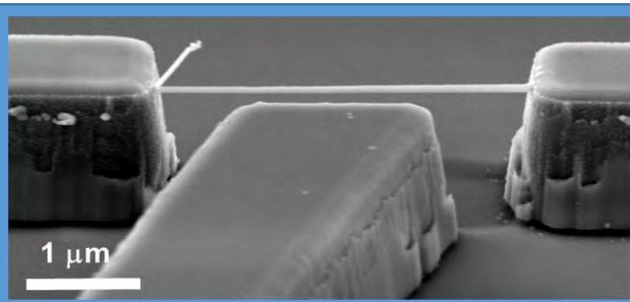
Logic Circuits with Carbon Nanotube Transistors

Bachtold et al. Science. 2001

Silicon nanowire resonators

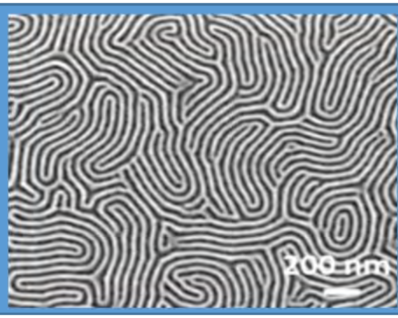
Sansa et al. Nature comm 2014.

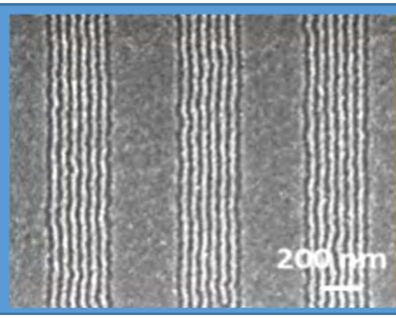




Block copolymer self-assembly

Oria et al. Microelectronic Engineering 2006

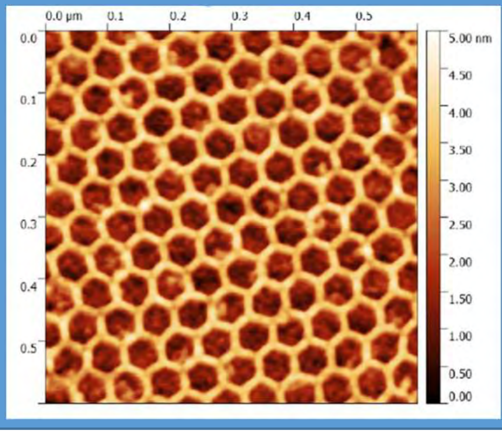




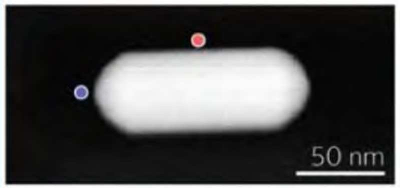
Assembly of DNA

DNA Origami

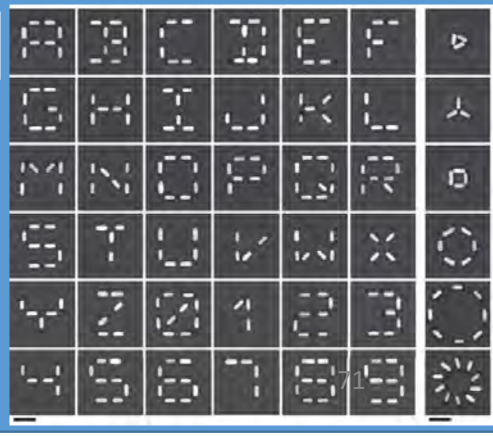
P. Wang et al. J.Am.Chem.Soc. 2016.



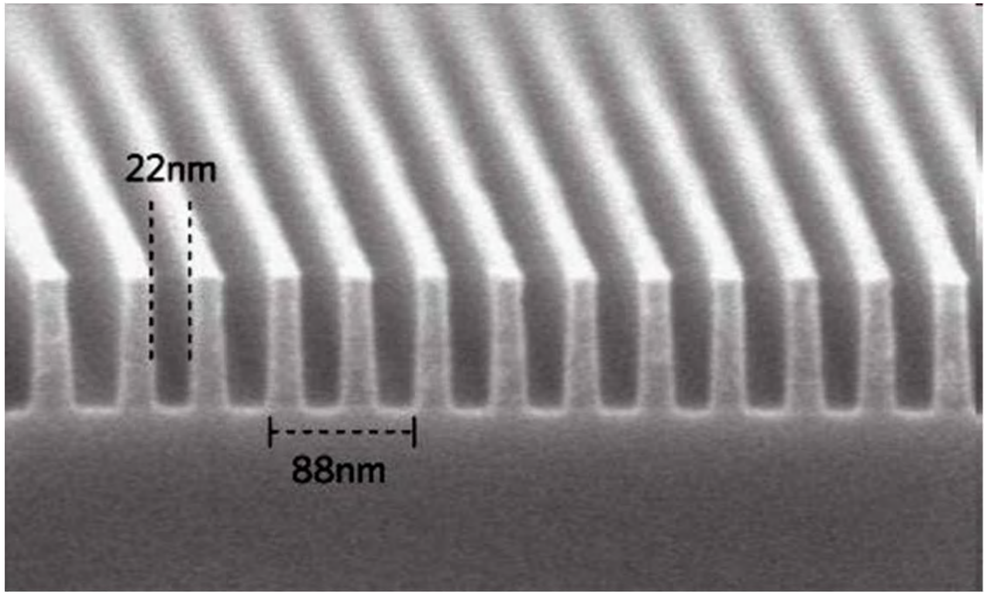
Assembly of nanocrystals



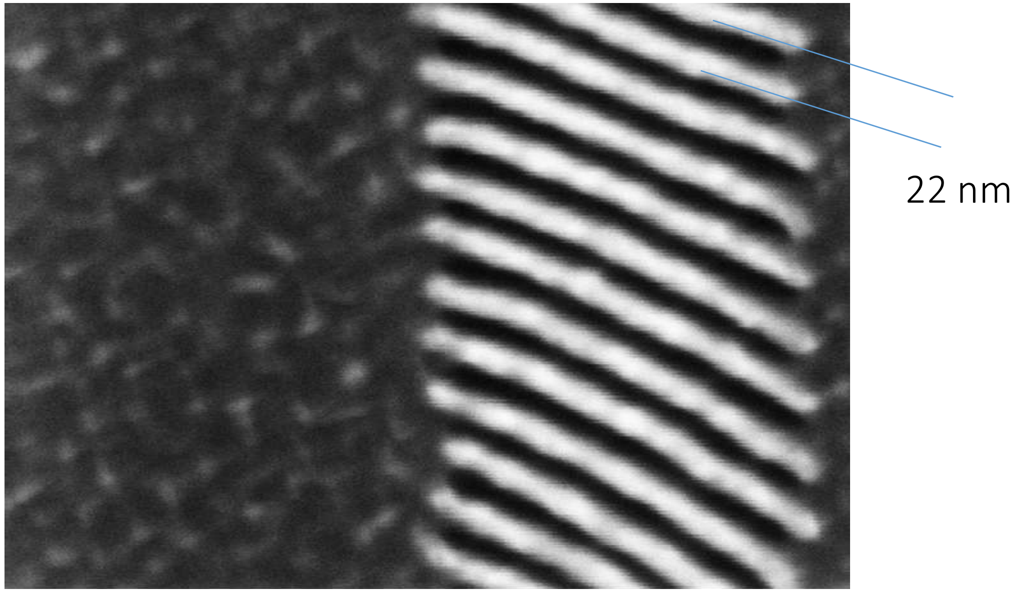
Flauraud et al. Nat.Nanotech. 2016



Directed self-assembly of block copolymers

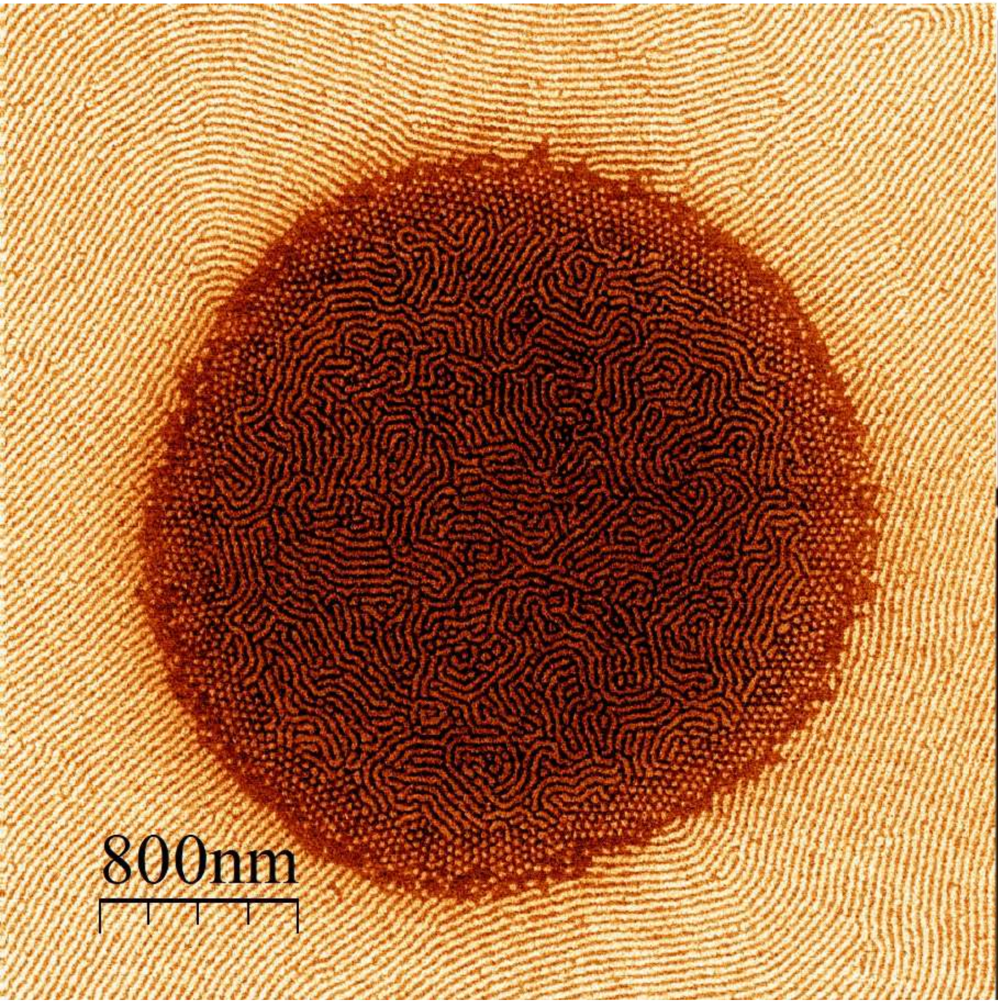


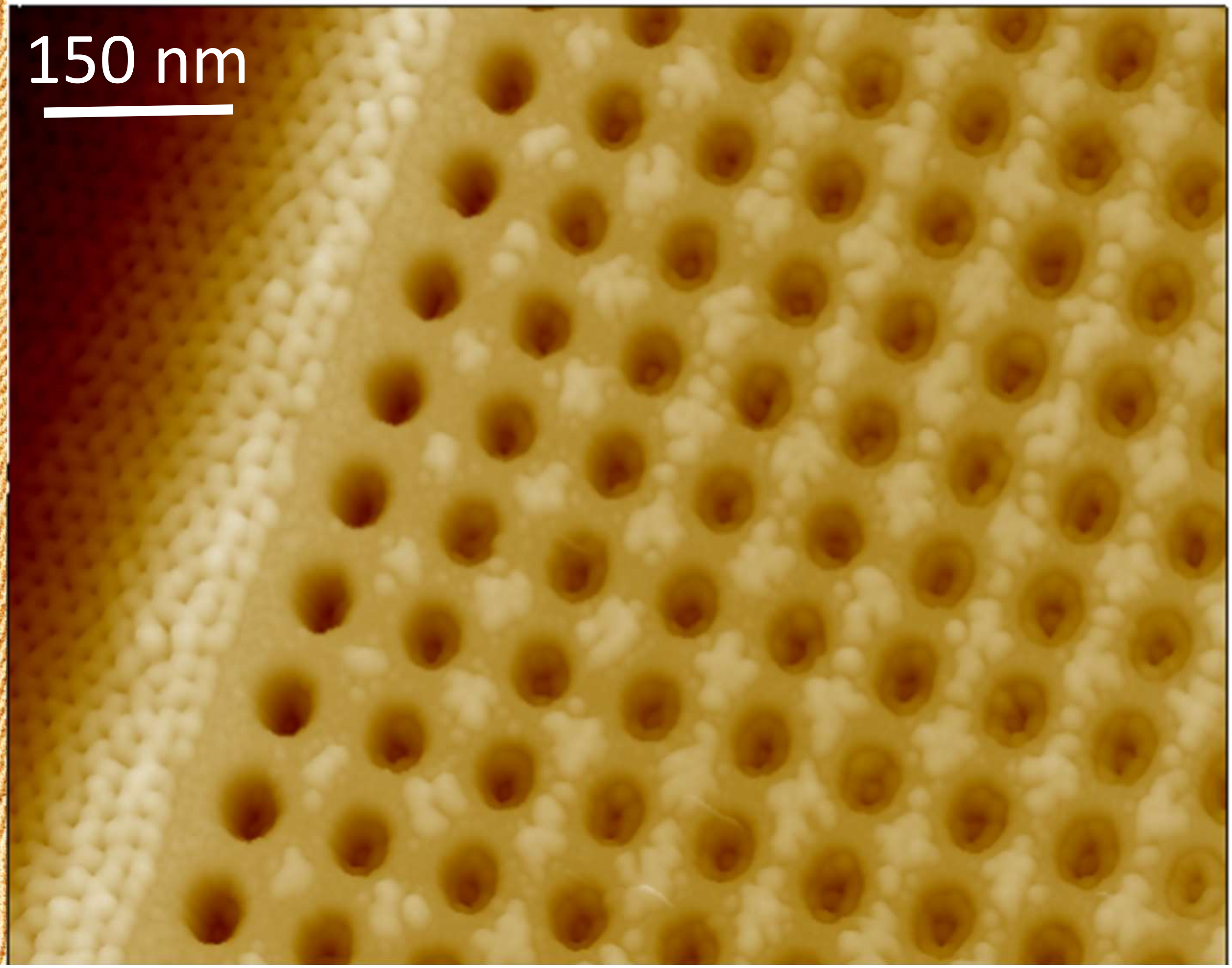
By optical lithography



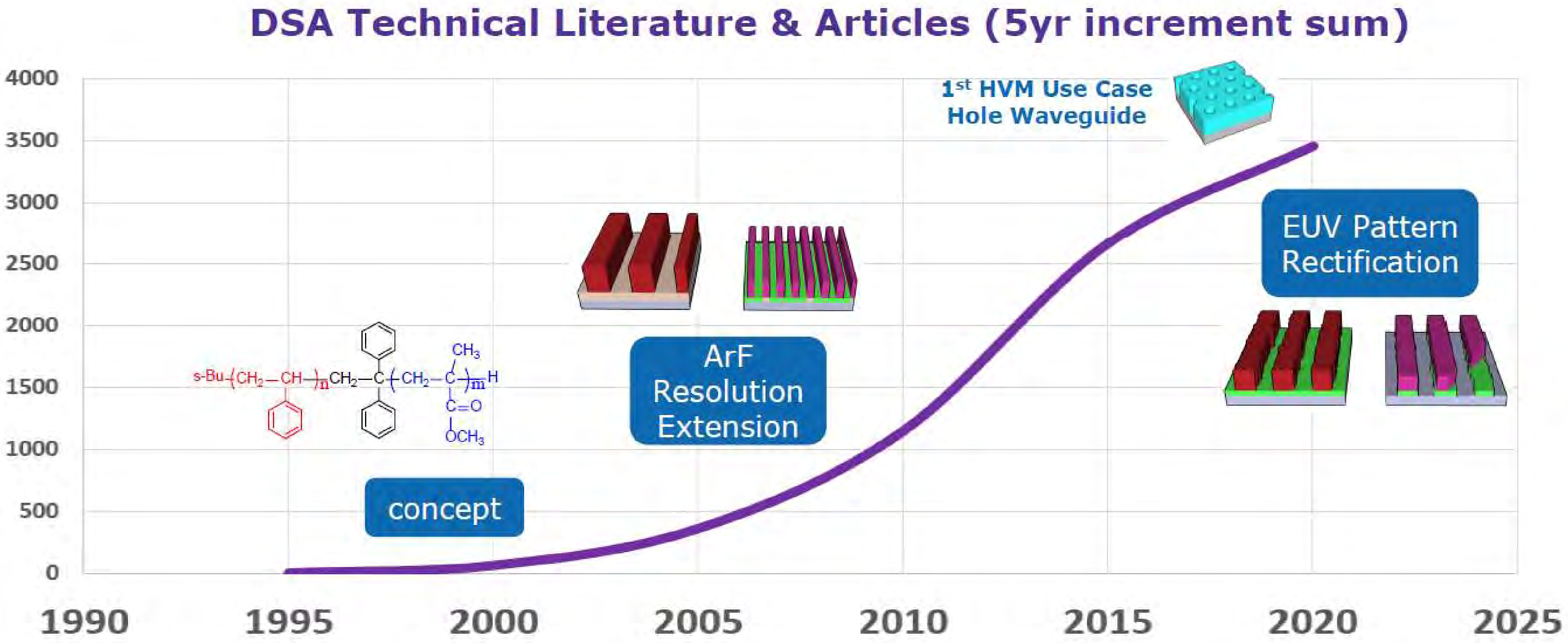
By directed sef-assembly of block copolymers

Directed self-assembly of block copolymers



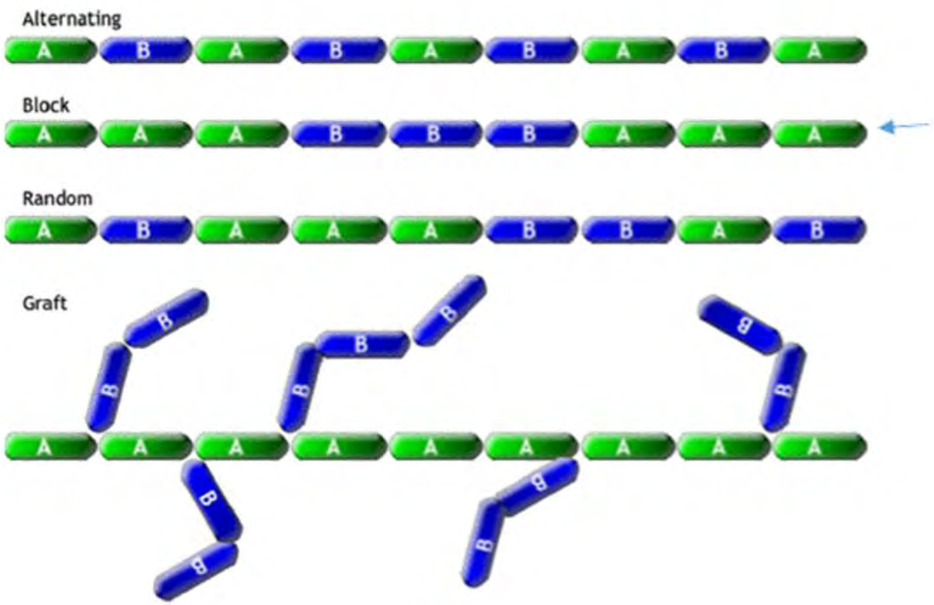


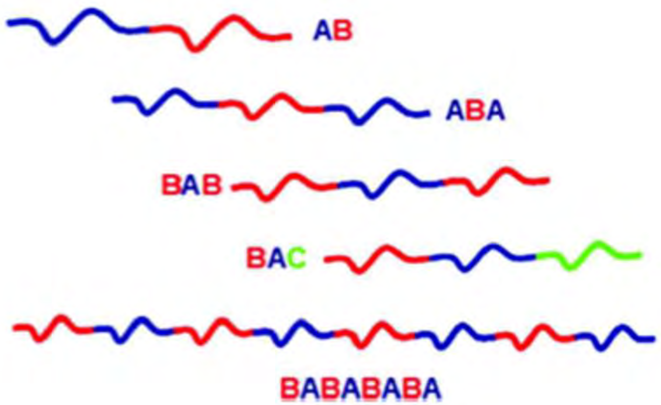
Historical Context
Directed Self-Assembly Applications

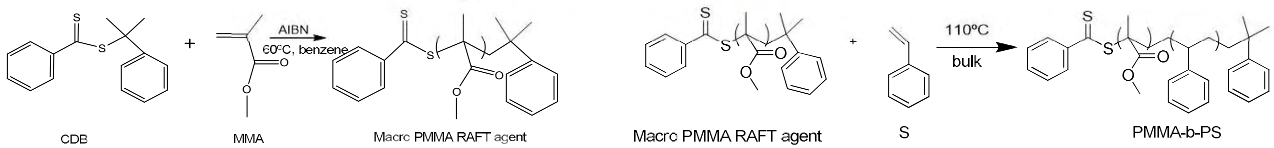


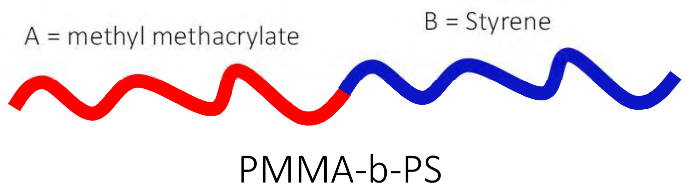
BLOCK CO-POLYMER

When two or more different monomers unite together to polymerize, their result is called a co-polymer and the synthetizing process is called co-polymerization. A block copolymer can be thought of as two or more distinct homopolymers linked end to end through covalent bonds. The number of distinct homopolymer homogeneous sections determines the molecular architecture of block copolymer; diblock, triblock, and higher multiblock copolymers are possible





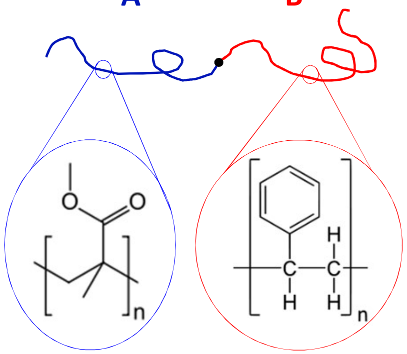




Ho-Cheol Kim et al. Block Copolymer Based Nanostructures: Materials, Processes, and Applications to Electronics. Chem. Rev. 2010, 110, 146-177

BLOCK CO-POLYMER SELF-ASSEMBLY

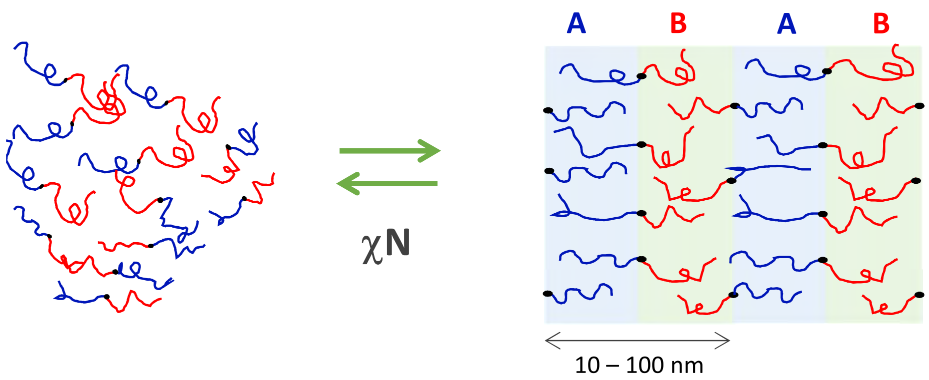
- ***What are block copolymers?***



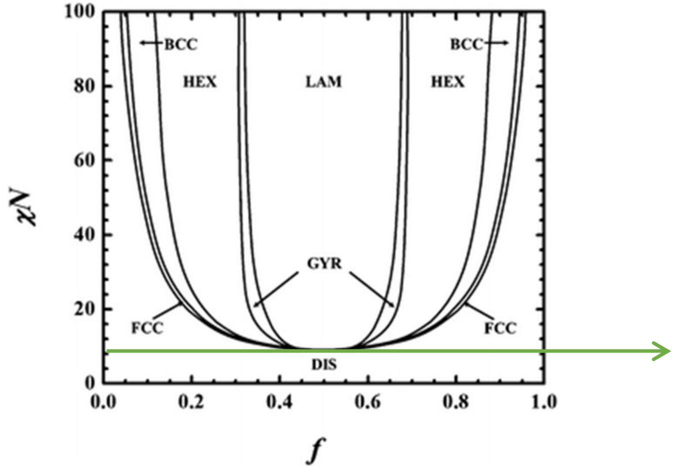
f: Volume fraction of one block in a BCP

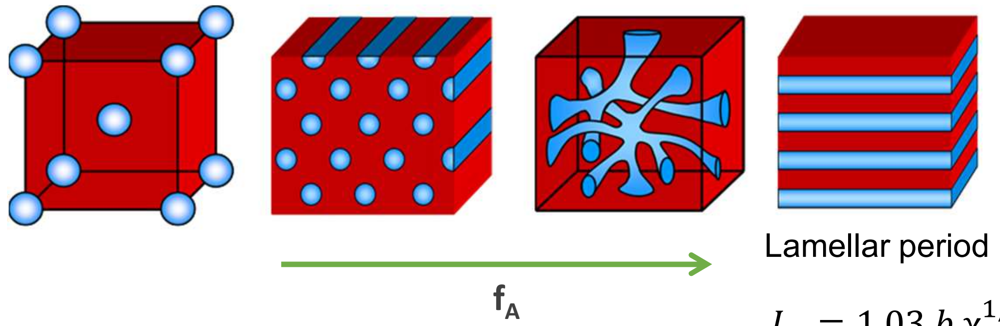
χ: Flory-Huggins interaction parameter

N: Polymerization index



- ***Phase diagram of A-B diblock copolymer***



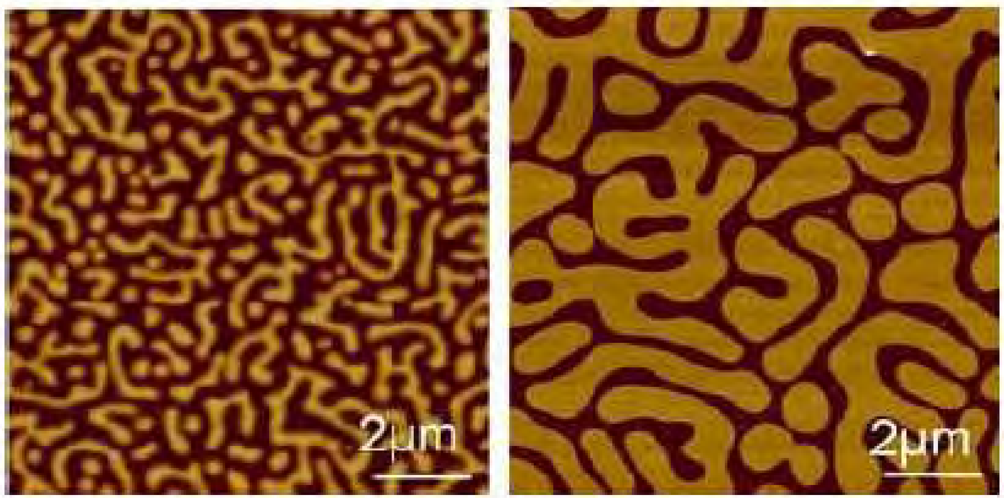


$$L_0 = 1.03\, b\, \chi_{AB}^{1/6}\, N^{2/3}$$

Bates, F.S. and Fredrickson, G.H. "Block Copolymers – Designer Soft Materials", Physics Today, 52, 2 (1992)

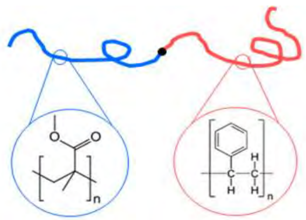
PHASE SEPARATION

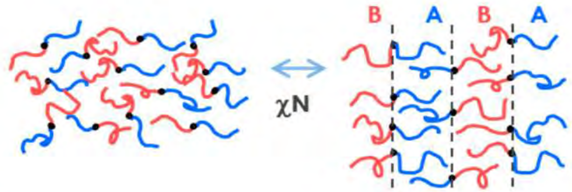
- **Macrophase-separation of homopolymer blends**
  - Immiscible polymer demix
  - Occurs on the micron-scale
  - The resulting phase separated polymeric domains are generally larger than the length of polymer chain and have not peculiar morphology



R. Pugin et al. J. Photopolymer Science and tech. 2009

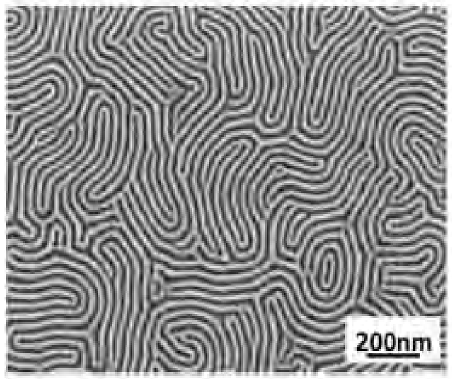
- **Microphase-separation of block copolymers**
  - Immiscible blocks demix
  - Occurs on the nanoscale, since the two blocks are covalently bound

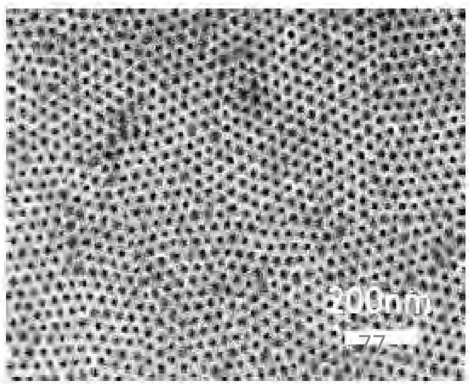




Disorder-order transition

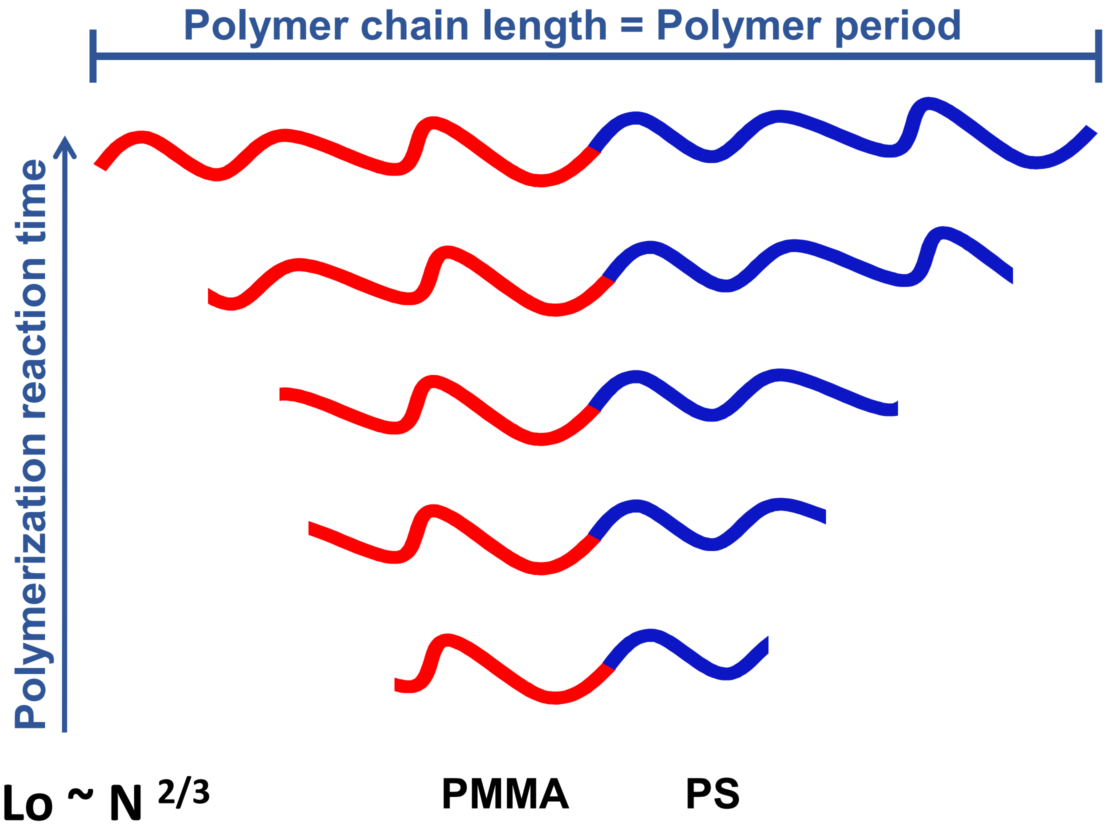
f: Volume fraction of one block in a BCP
N: Polymerization index
χ: Flory-Huggins interaction parameter



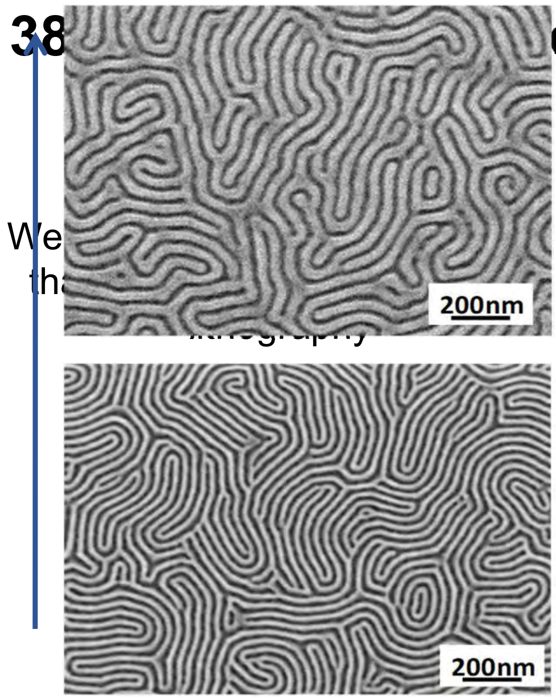


BLOCK CO-POLYMER SELF-ASEMBLY: HALF PITCH SIZE SETTING

<u>The pitch depends on the molecular weight and the CD uniformity depends on the polidispersity index</u>

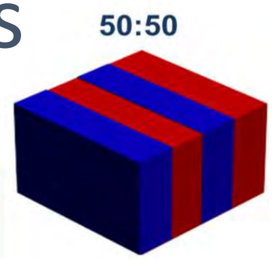


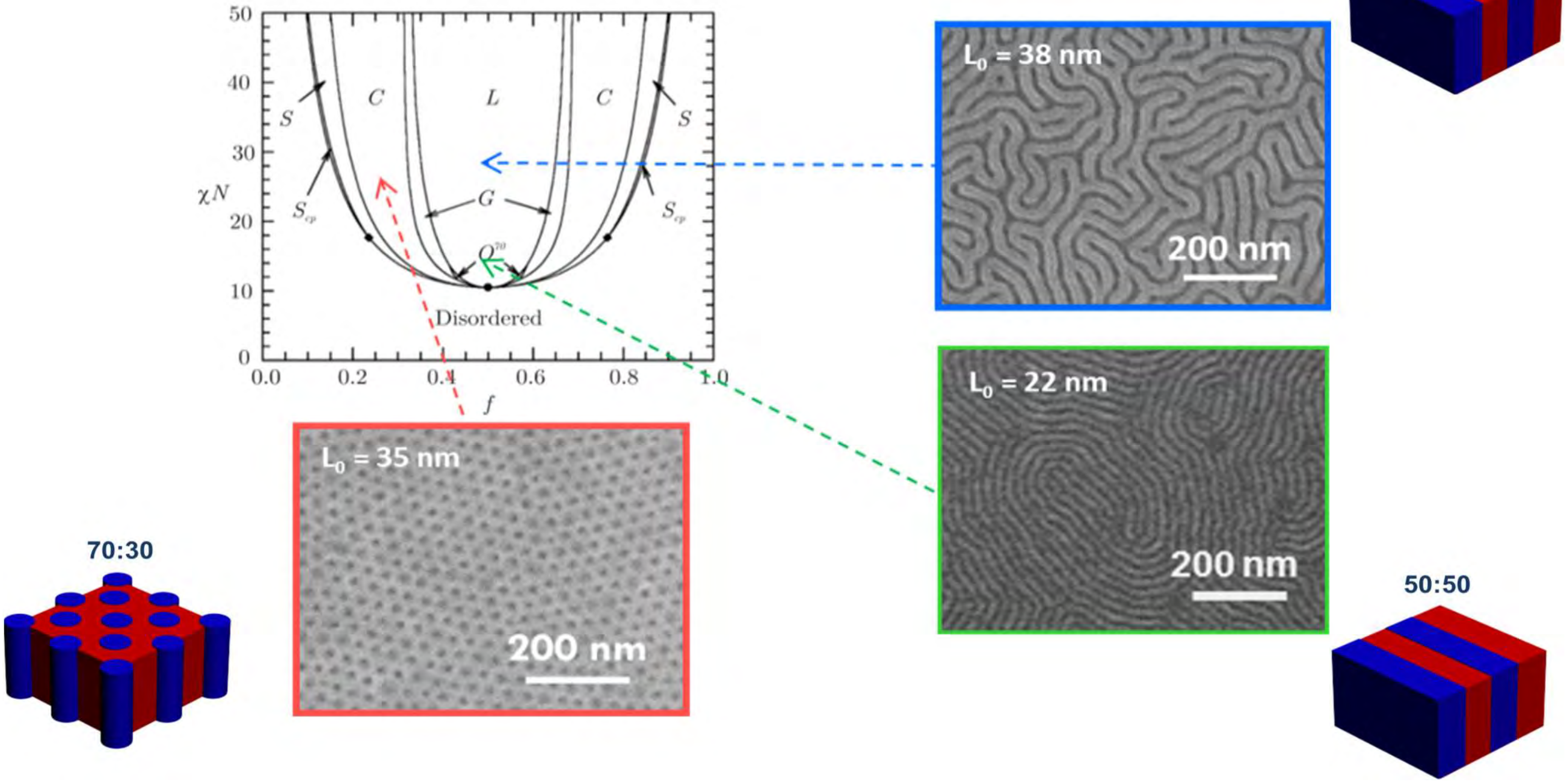
Mn = 45 kg/mol & 1.12 PDI



Lo ~ N $^{2/3}$

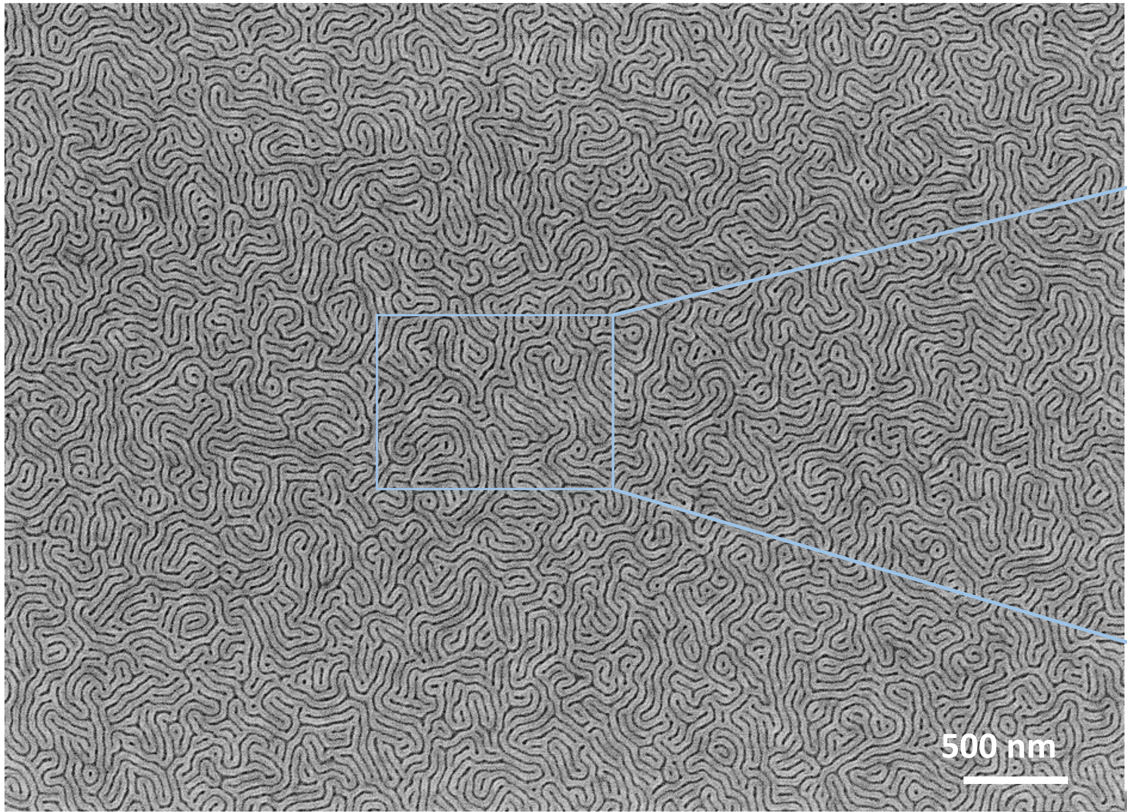
Morphologies of diblock copolymers

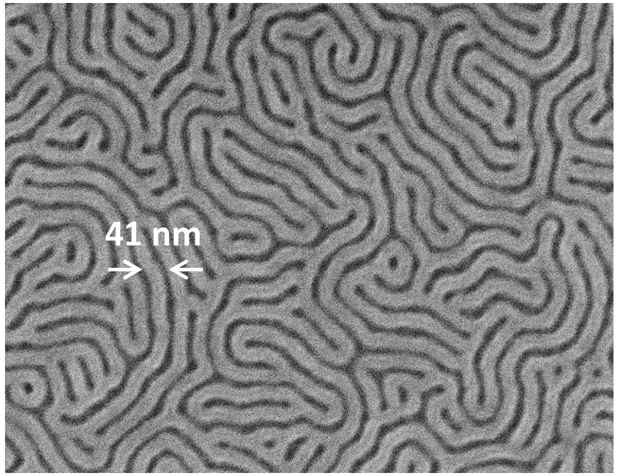


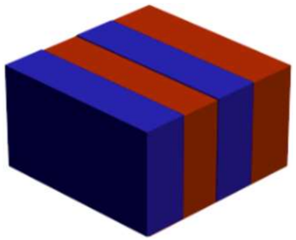


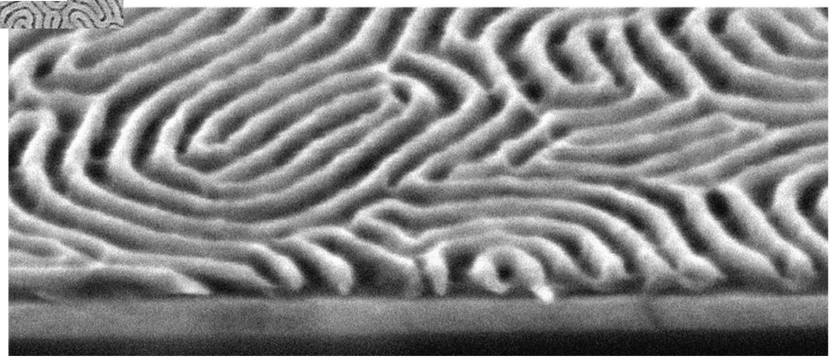
Bates, F.S. and Fredrickson, G.H. "Block copolymer thermodynamics: Theory and experiment", *Annu. Rev. Phys. Chem.*, 41 (1990)

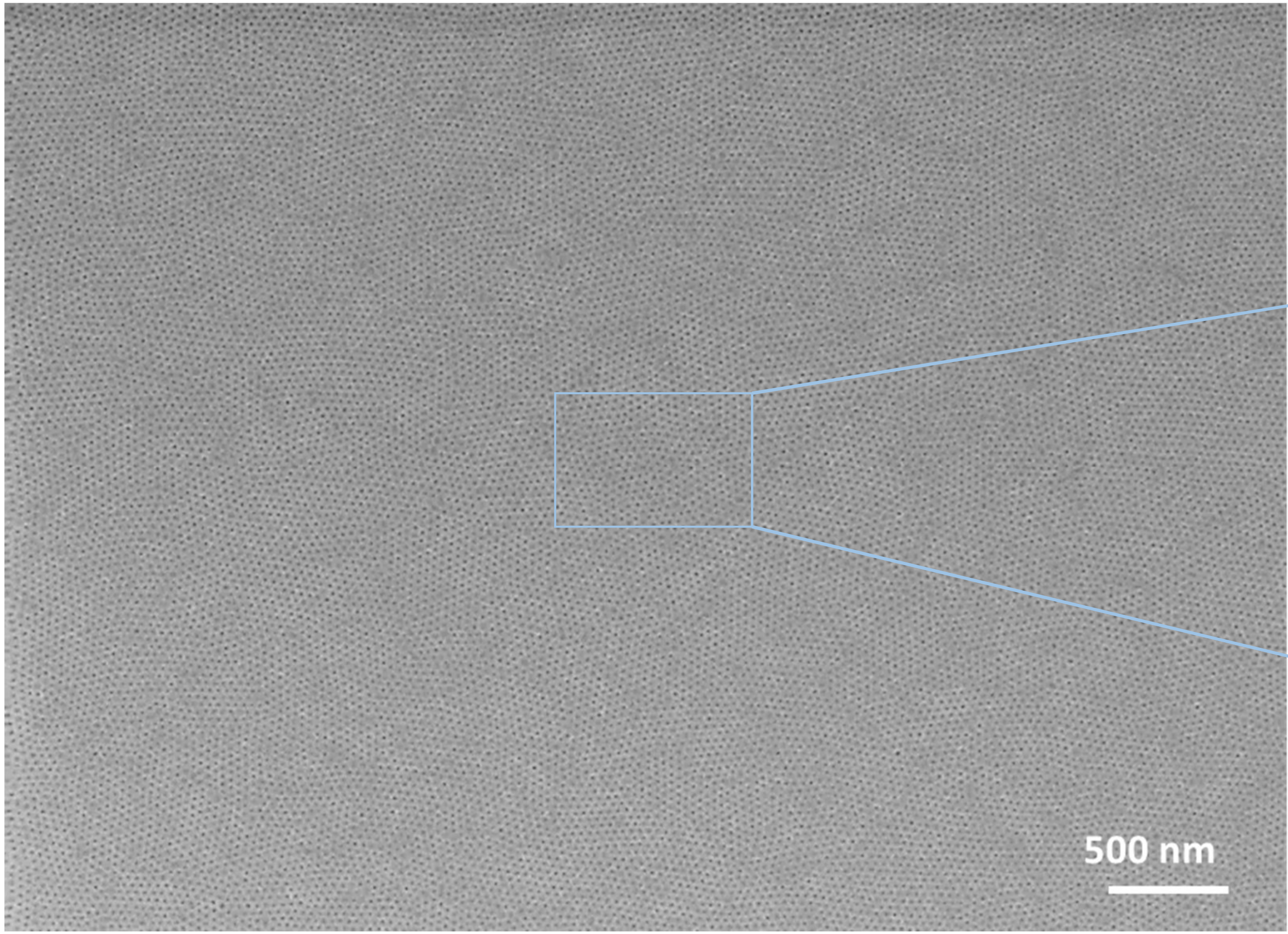
Examples of phase segregation
Lamellar forming block copolymers



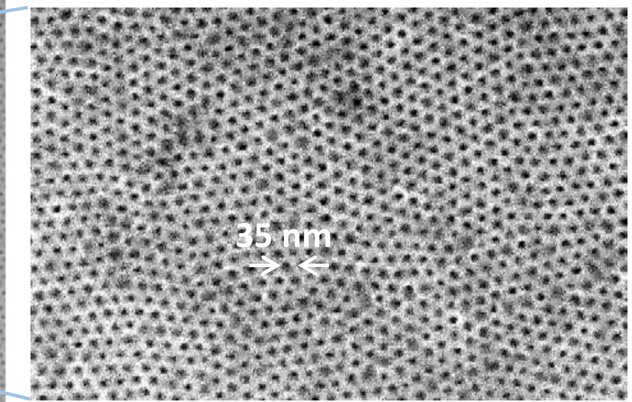


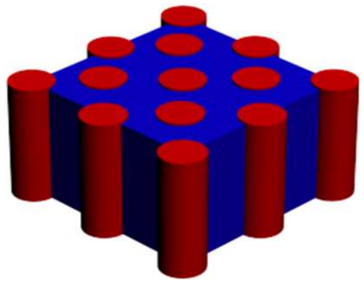






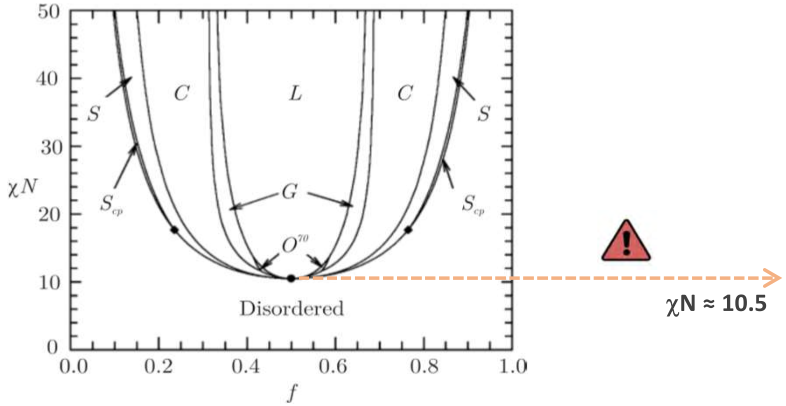
Cylindrical forming of block copolymers





High-χ block co-polymers

Motivation: DSA processes and materials **to scale to 5 nm** with potential to fulfill the future requirements of microelectronics industry



PS-*b*-PMMA
χ ≈ 0.04

Resolution limit: 11 nm

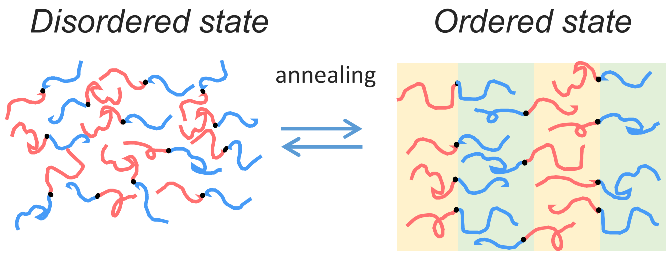
Organic BCPs		Inorganic BCPs	
BCP system	χ value	**BCP system**	χ value
PS-b-PMMA	0.041	**PS-b-PFS**	0.08
PS-b-PEO	0.077	**PS-b-PDMS**	0.26
PS-b-P2VP	0.178	**PTMSS-b-PLA**	0.46
PS-b-PLA	0.233	**PS-b-MH**	0.58
PS-b-PI	0.110	**PLA-b-PDMS-b-PLA**	1.4

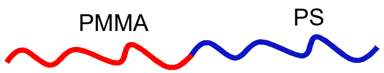
Organic high- χ materials
- Low etching contrast between blocks
- Not very high- χ values

Inorganic high- χ materials
- High etching contrast between blocks
- High- χ values

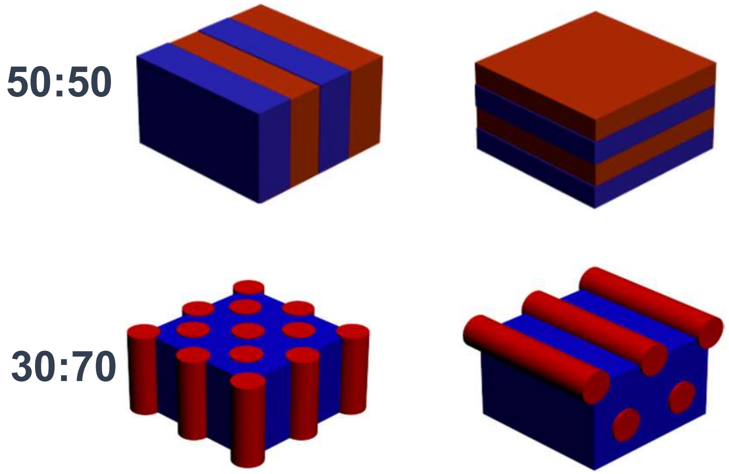
Each block copolymer requires the proper neutralization layer

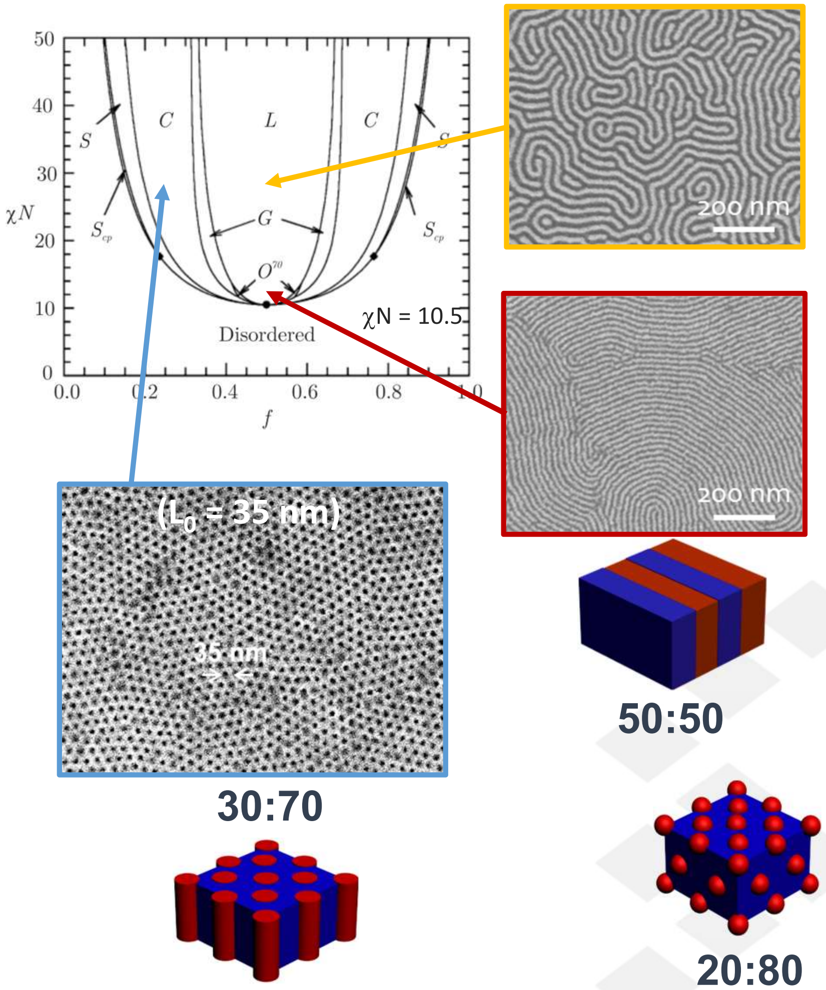
PHASE SEPARATION AND SURFACE/INTERFASE ENERGY



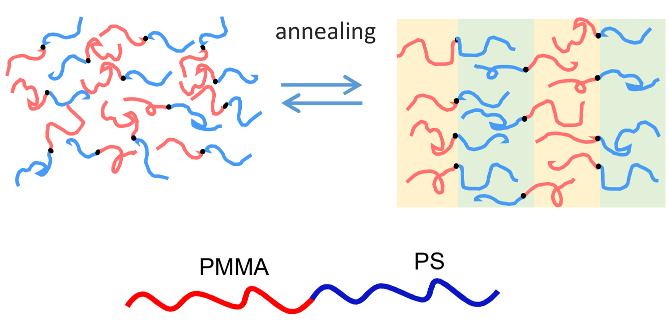


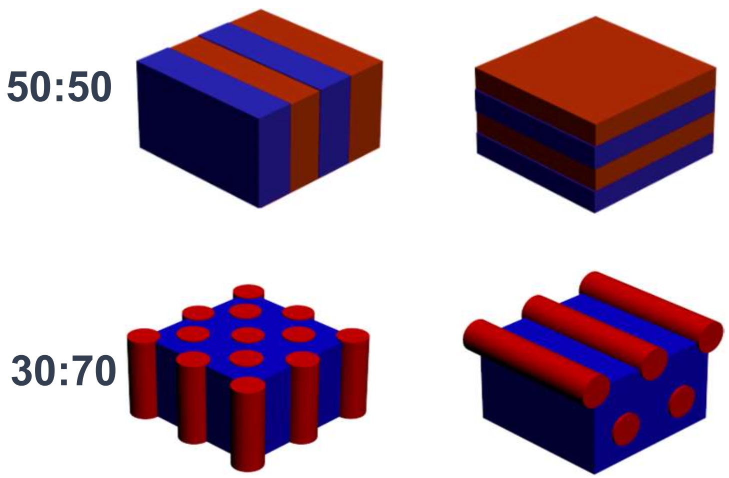
Neutral surface | **Non-neutral surface**



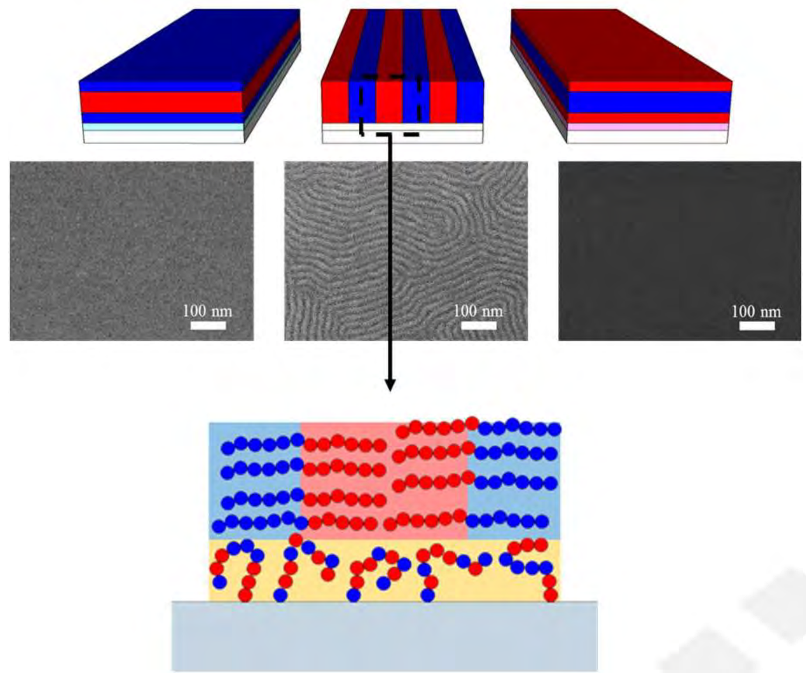


Thin film preparation of block co-polymers

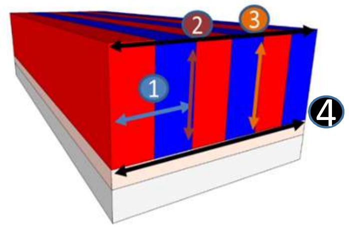




The **surface affinity** is controlled by a **Brush layer**



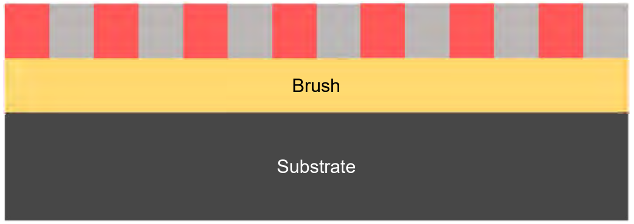
$$E_{tot} = \sum E = E_{stretch} + E_{curvature} + E_{interblock} + \boldsymbol{E_{surface}}$$



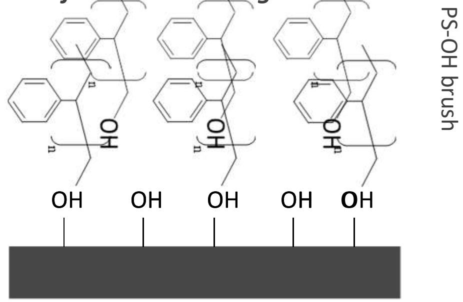
Surface neutralization

For technological applications there is the need to control the BCP morphology, and thus **avoid wetting morphologies** at the polymer-brush interface.

Use of **brush polymer** to create a neutral layer which balances the surface free energy between the BCP domains

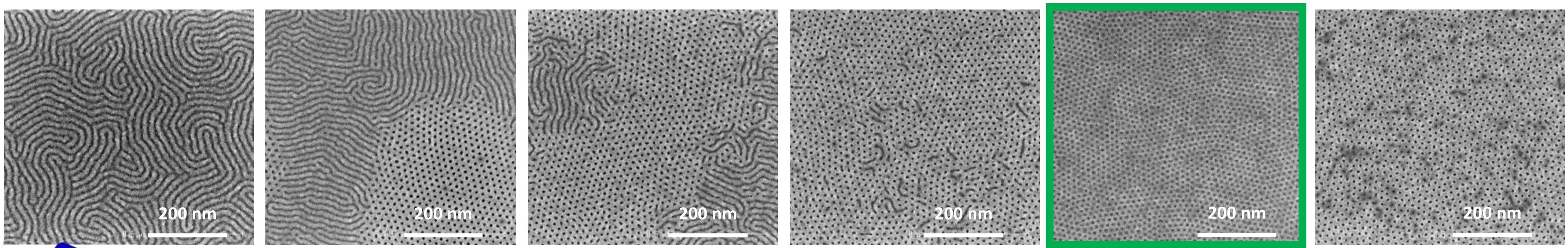


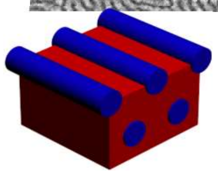
After the annealing treatment:

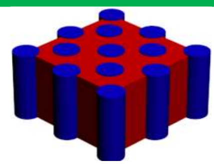


Mansky, P., "Controlling polymer-surface interactions with random copolymer brushes", Science, 275, 1458-1460 (1997)

% PMMA (PS-r-PMMA)







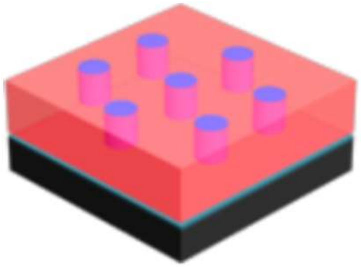
Cylindrical PS-b-PMMA

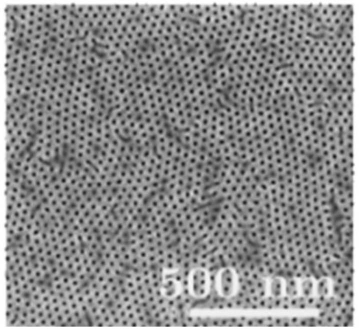
SEM images taken after PMMA removal

Block copolymer – surface interaction: *Role of surface affinity*

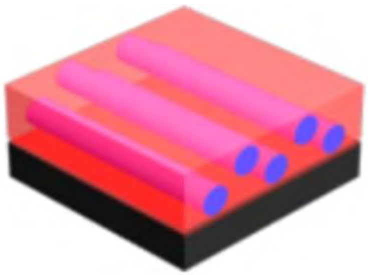
Interaction energies $E = \boxed{(E_{A/B} + E_{conf})} + \boxed{(E_{A/Subs} + E_{B/subs} + E_{A/air} + E_{B/air})}$

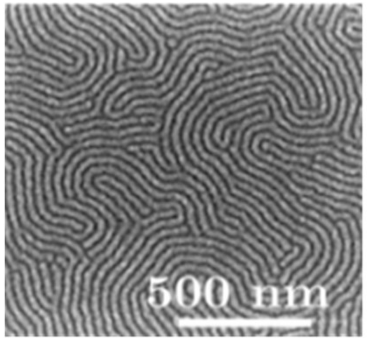
Neutral surface



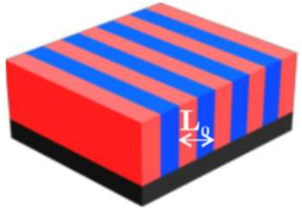


Affine surface





Neutral surface



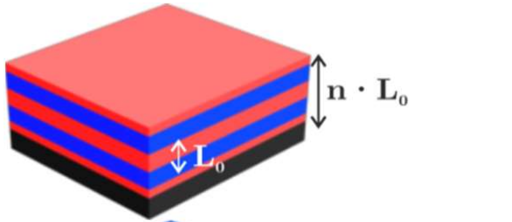
$\gamma_{A\text{-air}} \approx \gamma_{B\text{-air}}$

$\gamma_{A\text{-subs}} \approx \gamma_{B\text{-subs}}$

AFFINE SURFACE

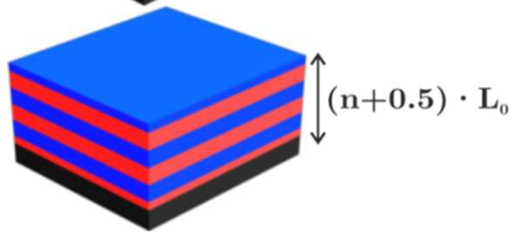
$\gamma_{A\text{-air}} < \gamma_{B\text{-air}}$

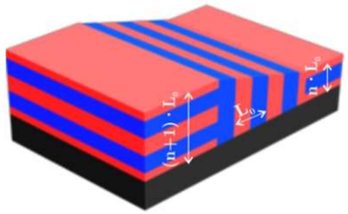
$\gamma_{A\text{-subs}} < \gamma_{B\text{-subs}}$

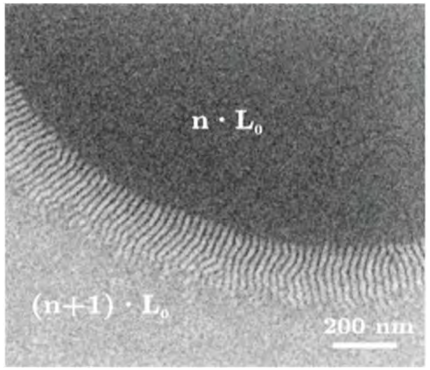


$\gamma_{A\text{-air}} > \gamma_{B\text{-air}}$

$\gamma_{A\text{-subs}} < \gamma_{B\text{-subs}}$

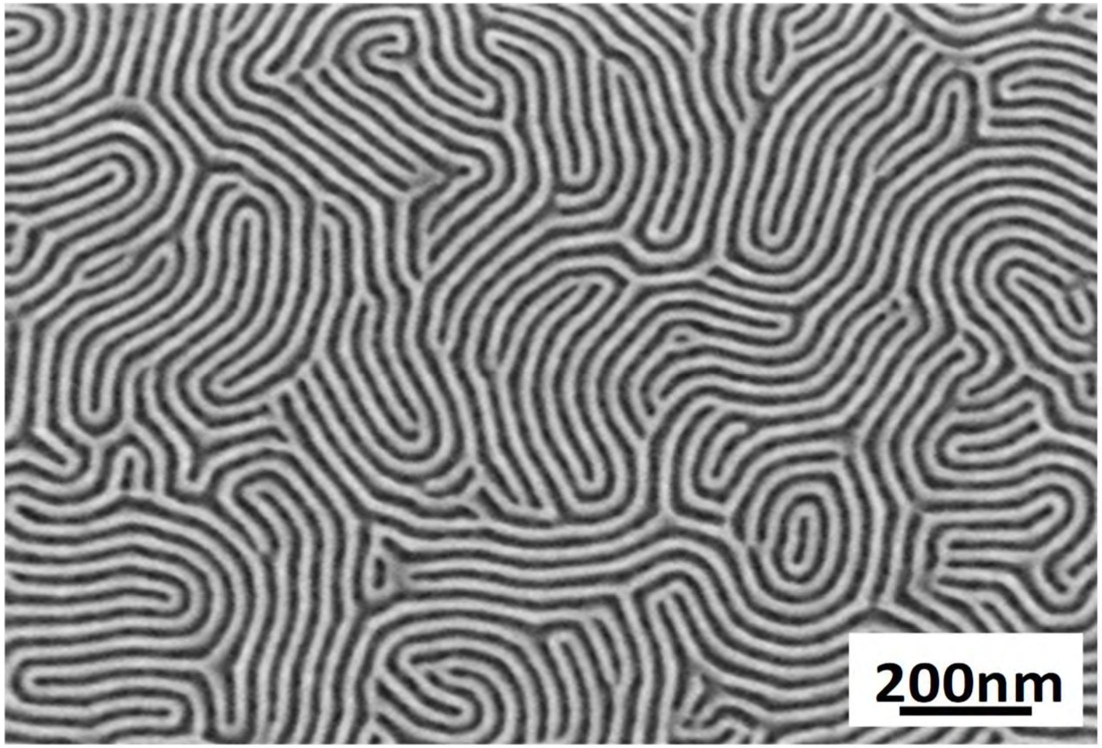


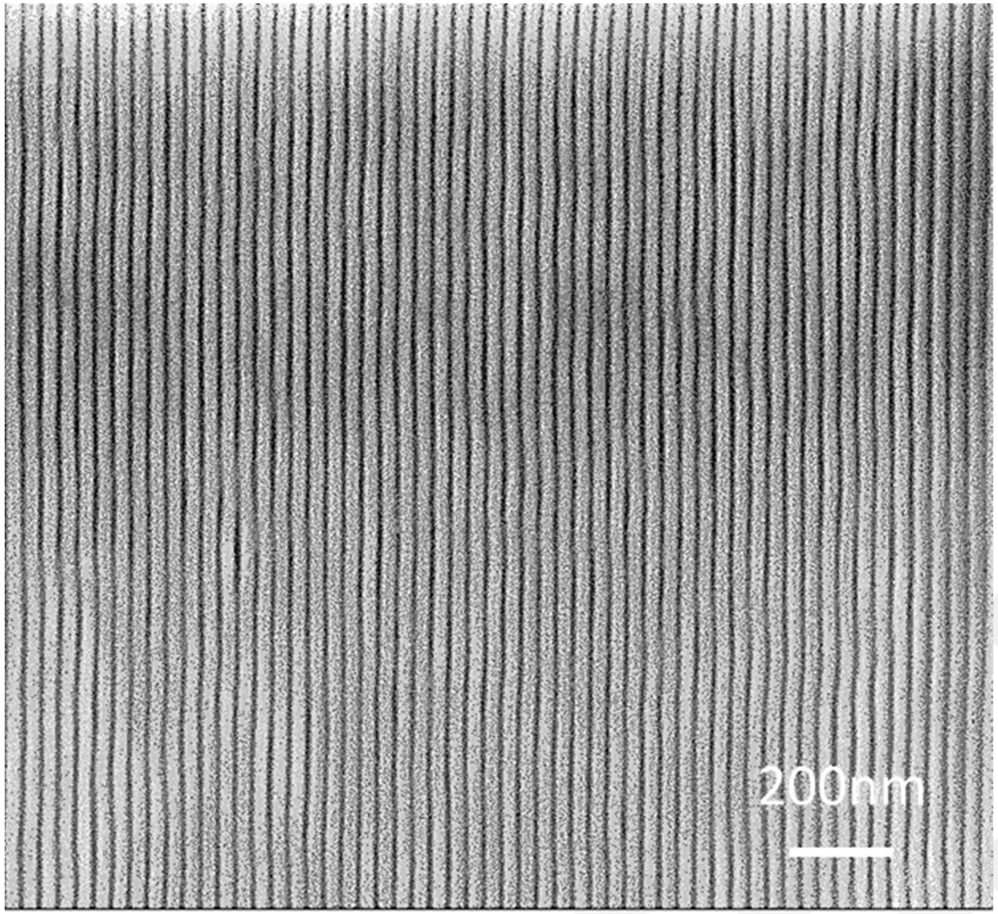




When the BCP **does not** fulfill the film thickness **commensurability** condition, the BCP tend to create some **holes** or **terraces**

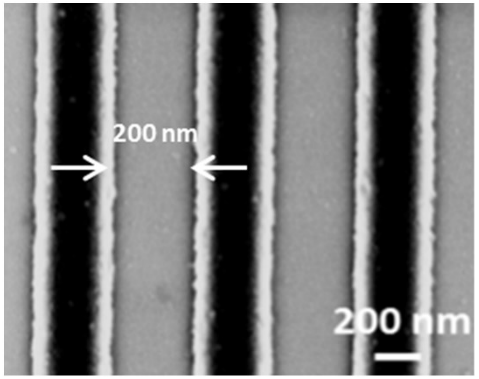
Directed Self-Assembly (DSA): Short-range order to long-range order





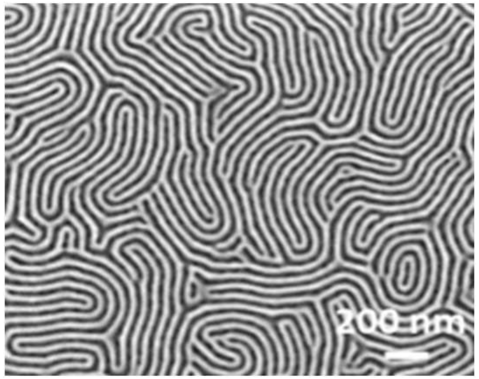
Directed self-assembly (DSA) methods

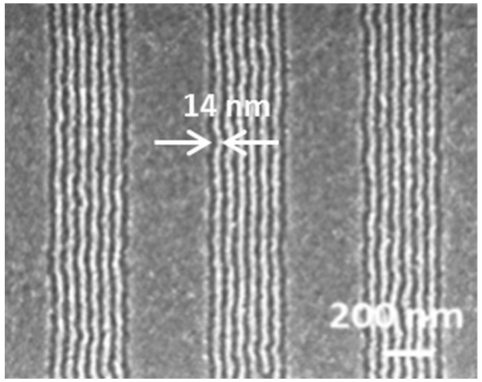
Conventional Lithographic methods



Guiding patterns

Block copolymer self-assembly

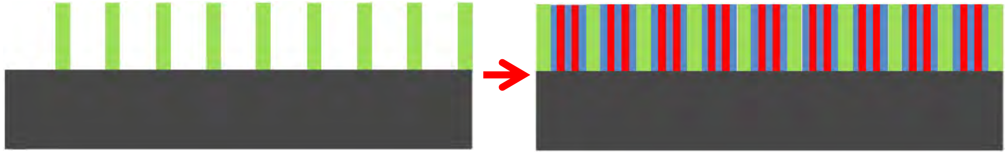




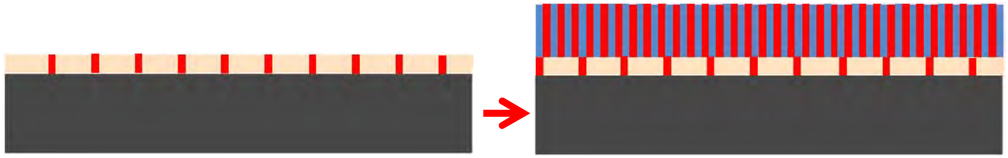
Directed Self-Assembly of Block Copolymers (DSA)

Methodologies to DSA

Graphoepitaxy



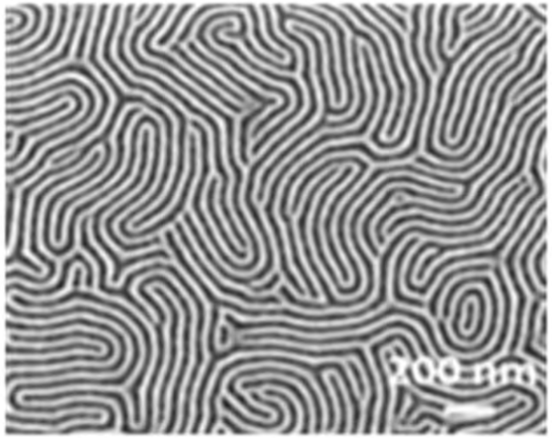
Chemoepitaxy



The density multiplication and pattern rectification are the main advantages of DSA, since they allow achieving dense patterns with tight size and placement tolerances, low defect densities and reduced e-beam writing times.

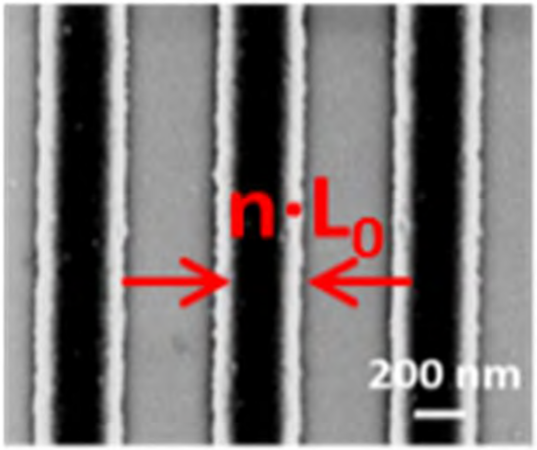
Directed self-assembly (DSA) methods

Density multiplication factor: n

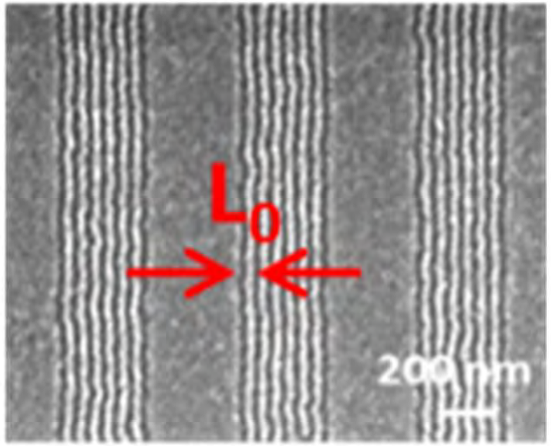


Intrinsic property of BCP to self-assemble

+

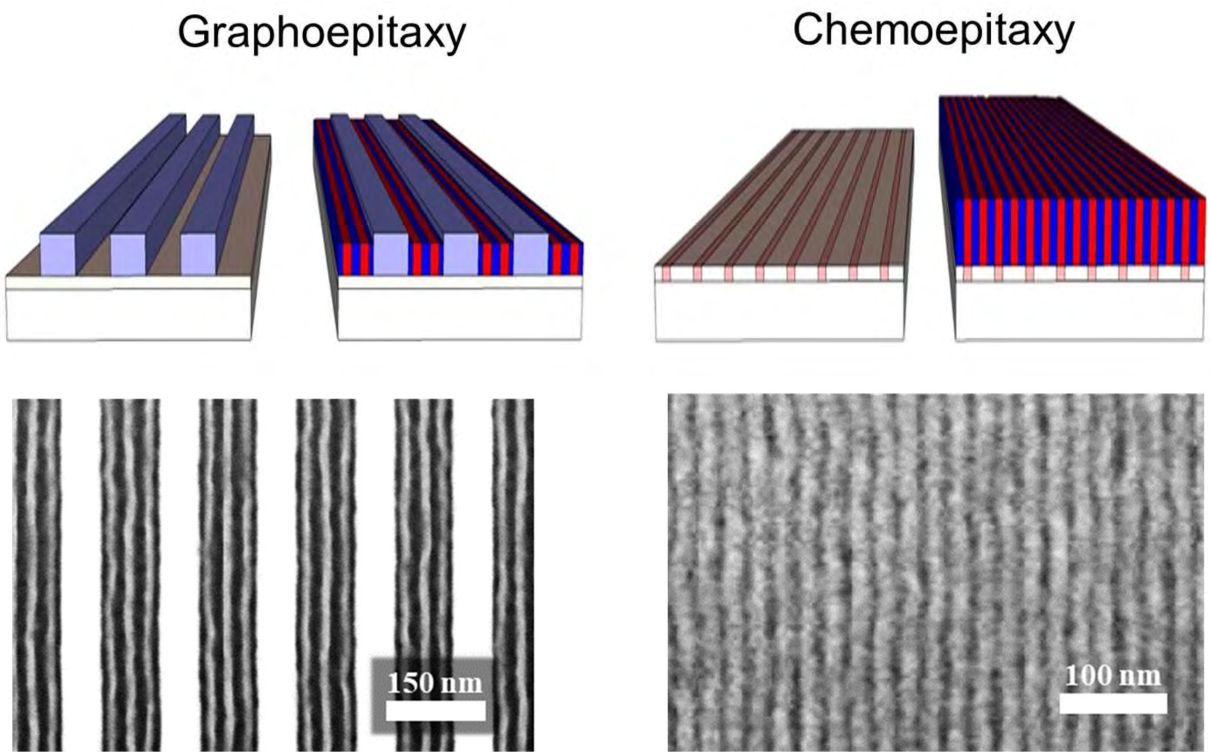


=



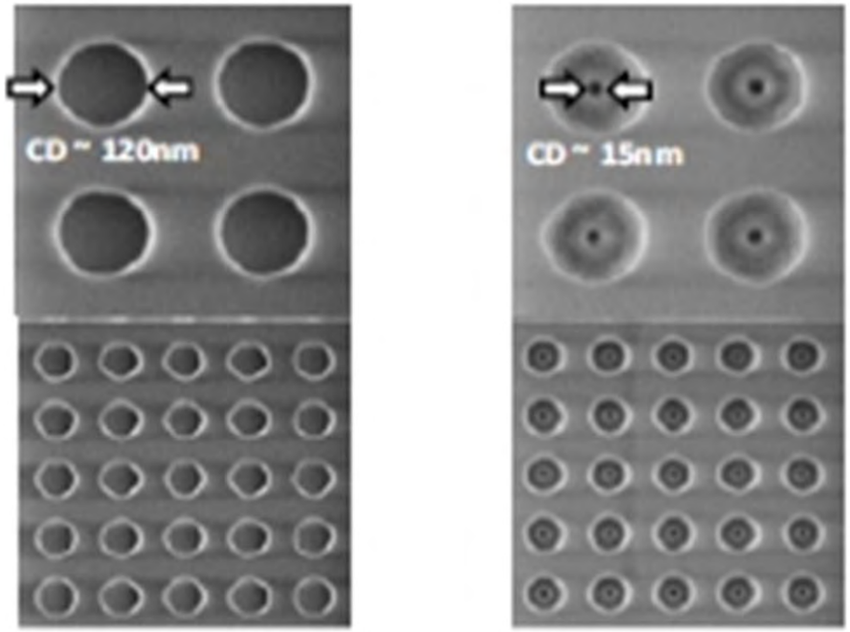
Directed self-assembly: guiding patterns

Line/space density multiplication



S. Gottlieb, D. Kazazis, I. Mochi, L. Evangelio, M. Fernández-Regúlez, Y. Ekinci, F. Perez-Murano SPIE Advanced Lithography, San José. (2017)

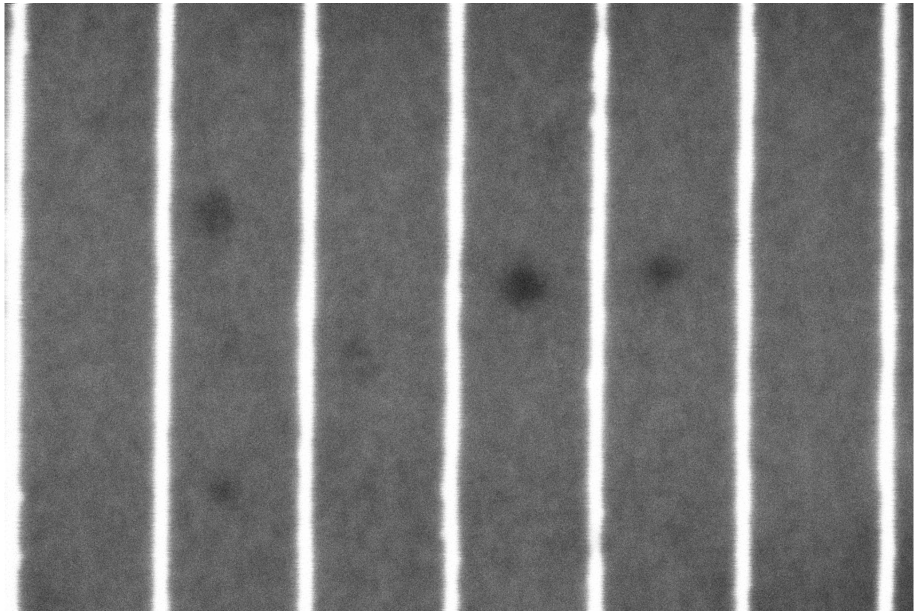
Contact shrink

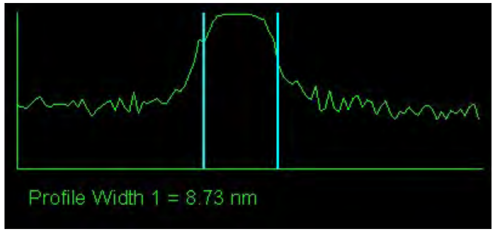


Tiron, R. et al. , "The potential of BCP's DSA for contact hole shrink and contact multiplication", Proc. SPIE, 8680, p. 868012 (2013)

DSA for line/space: high resolution guiding patterns

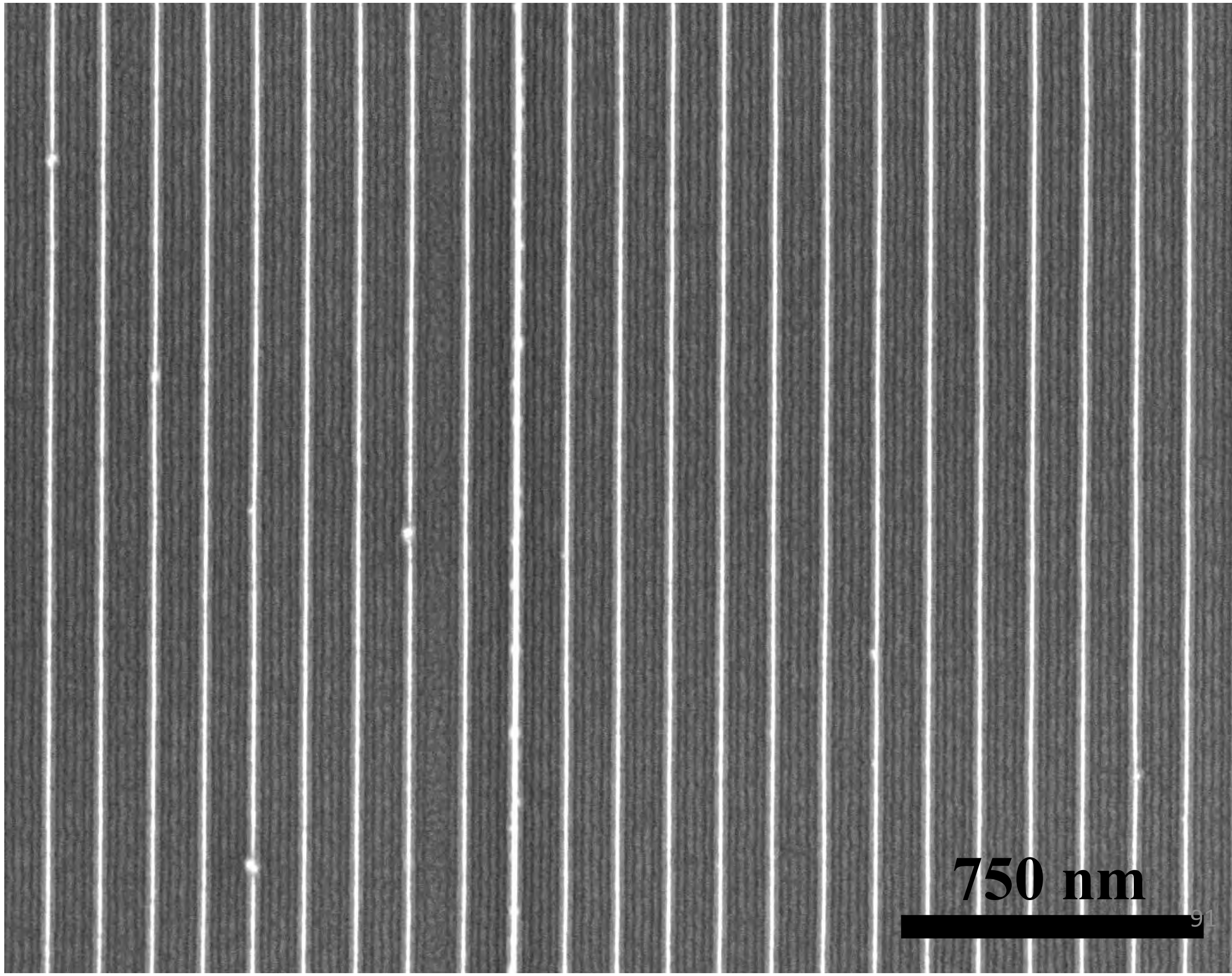
High resolution guiding patterns by EBL





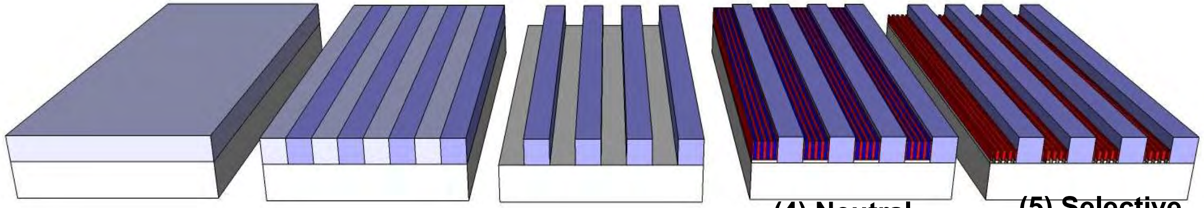
Sub-10 nm line width demonstrated
Pitch: 90 nm)

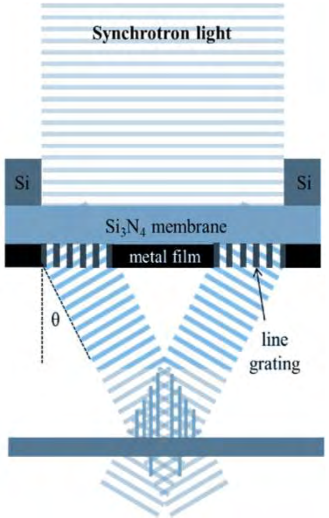
Gottlieb et al., 2018, Soft Matter, 14, 6799(808)

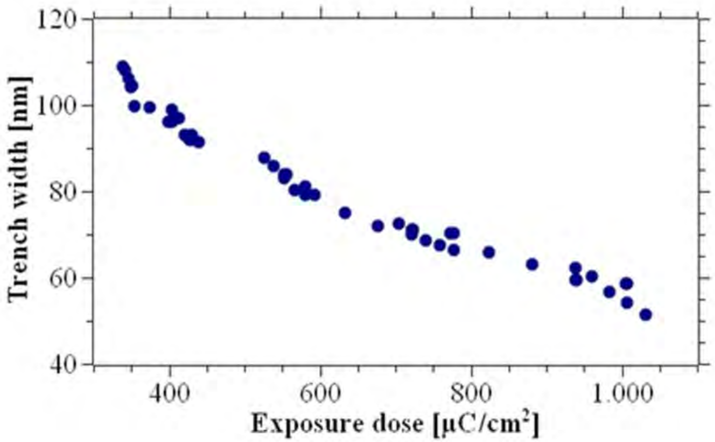


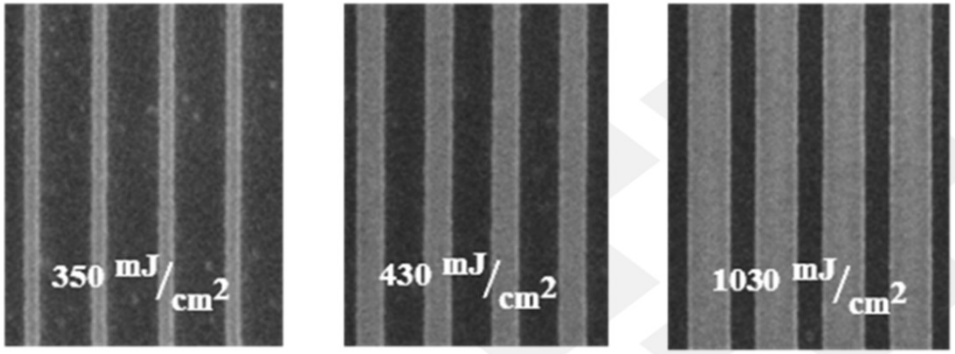
Nano-confinement and defectivity

Gottlieb et al., 2018, Soft Matter, 14, 6799(808)



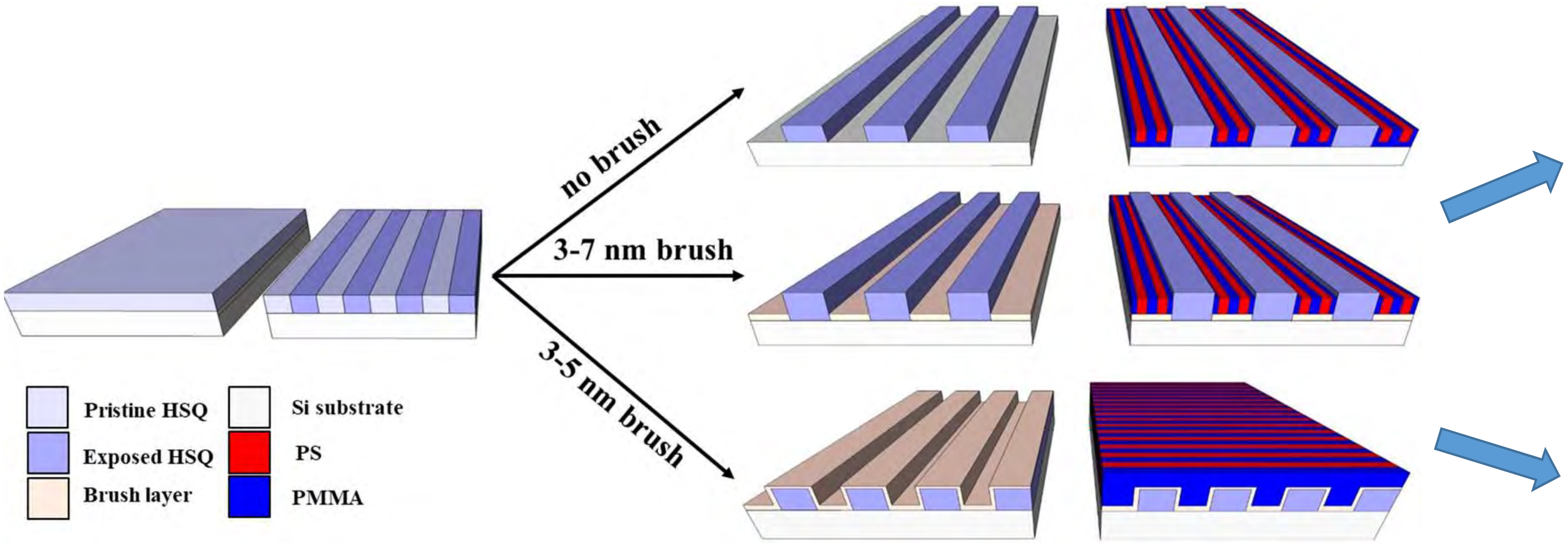


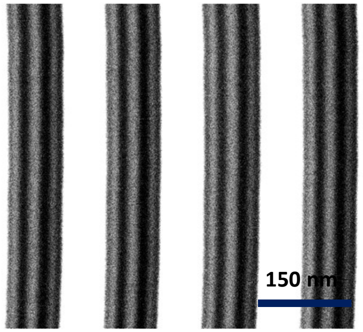




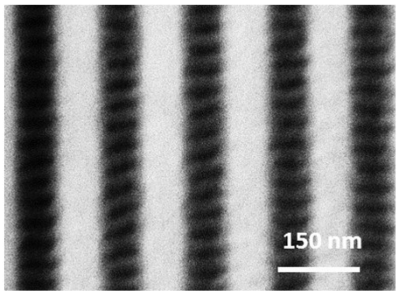
High resolution guiding patterns by EBL (i): Graphoepitaxy

IN DSA, the final morphology depends on theinteraction energy with the interfaces, which is achieved by covering the surfaces with an appropiate layer, usually a thin polymeric layer (brush)

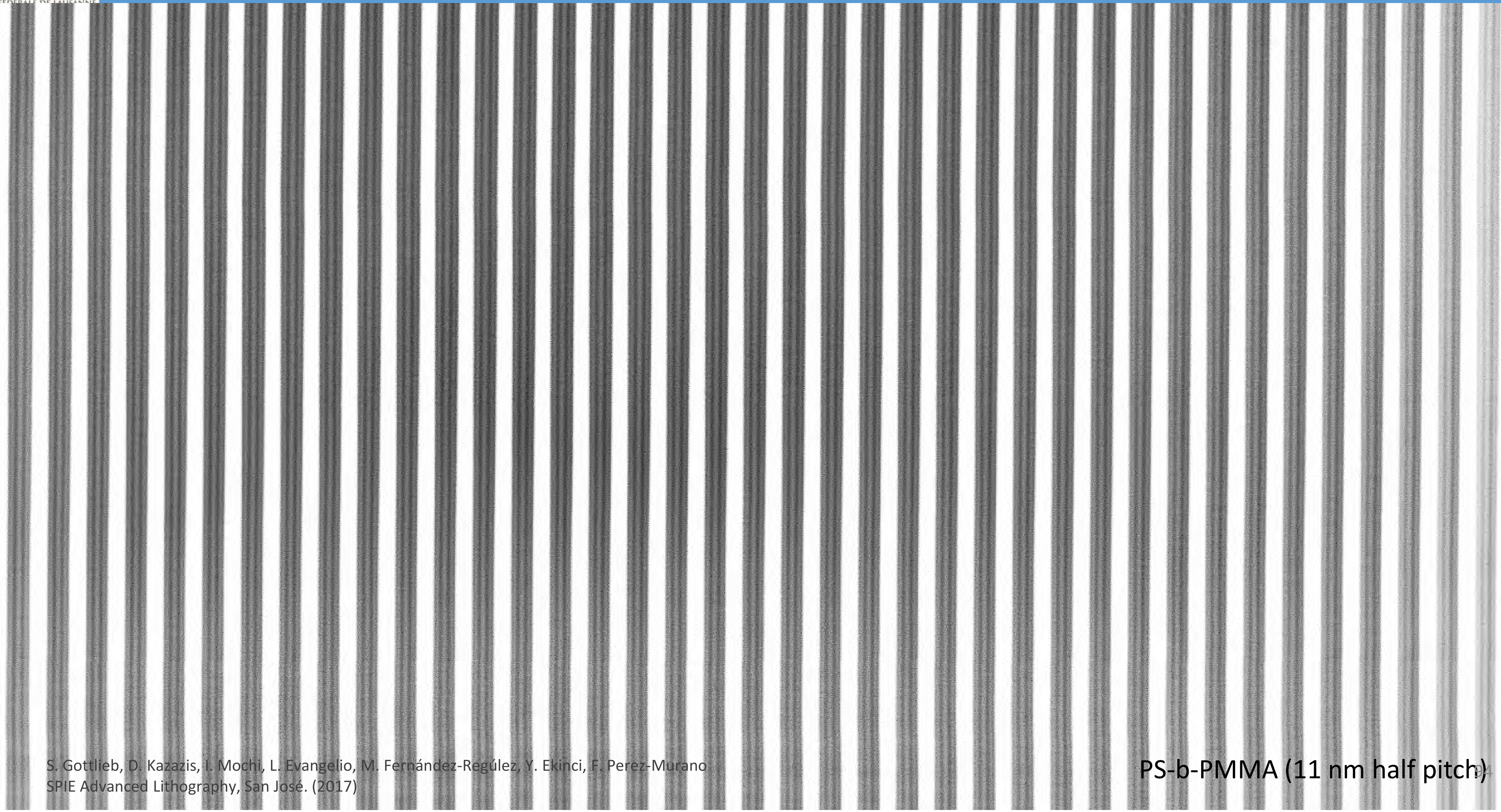




PS-b-PMMA (11 nm half pitch)



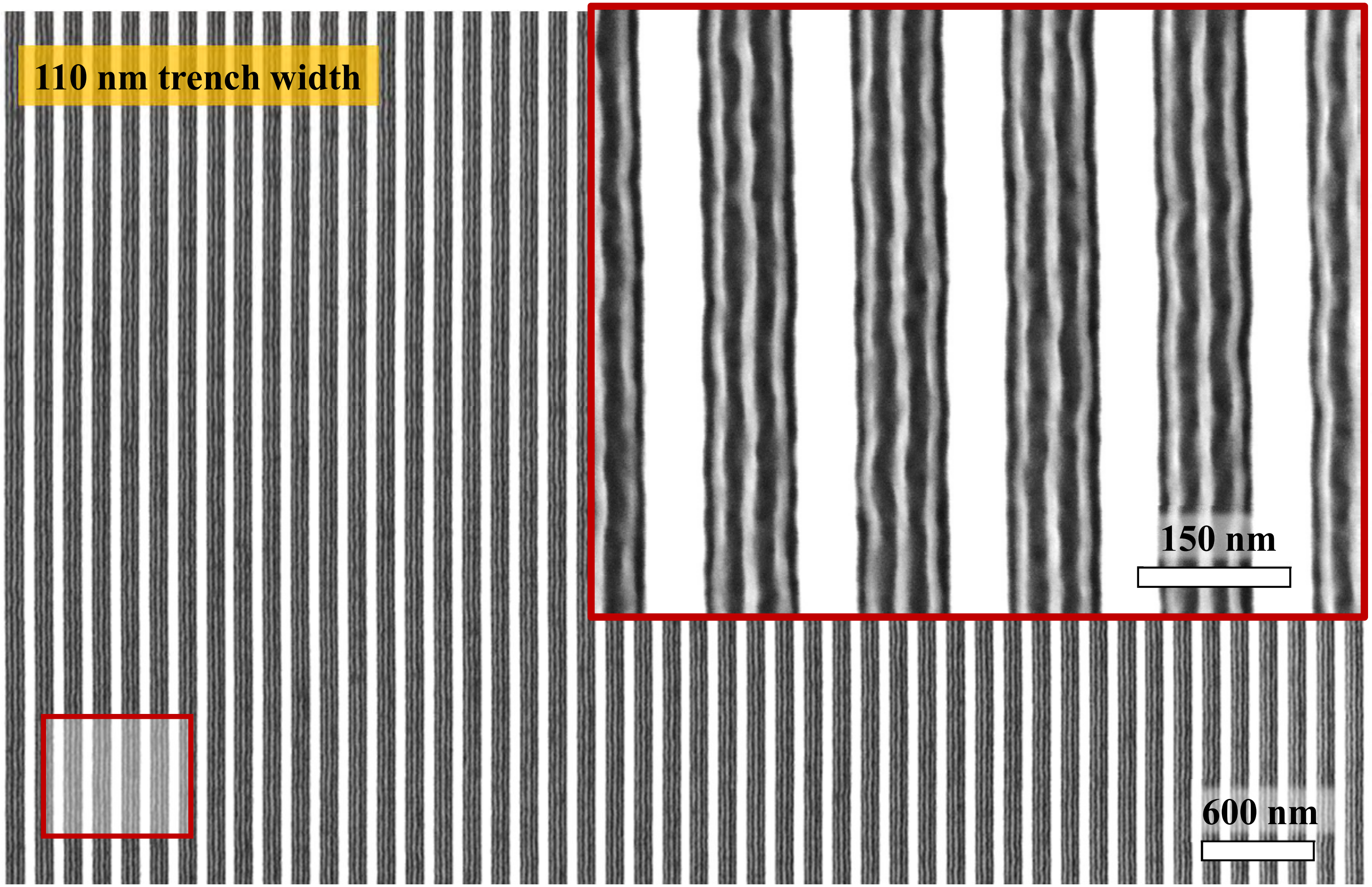
S. Gottlieb, D. Kazazis, I. Mochi, L. Evangelio, M. Fernández-Regúlez, Y. Ekinci, F. Perez-Murano. SPIE Advanced Lithography, San José. (2017)

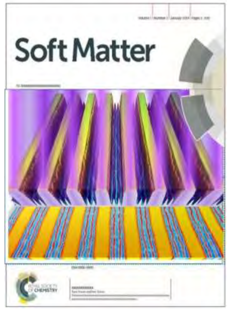


S. Gottlieb, D. Kazazis, I. Mochi, L. Evangelio, M. Fernández-Regúlez, Y. Ekinci, F. Perez-Murano
SPIE Advanced Lithography, San José. (2017)

PS-b-PMMA (11 nm half pitch)

Nano-confinement and defectivity

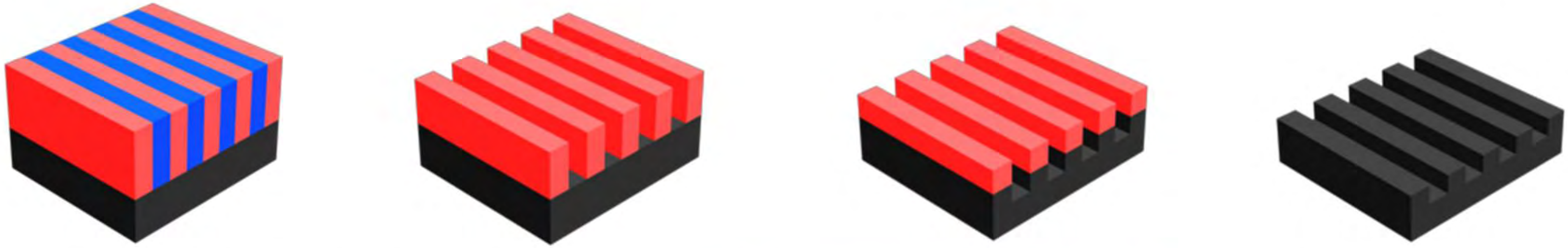


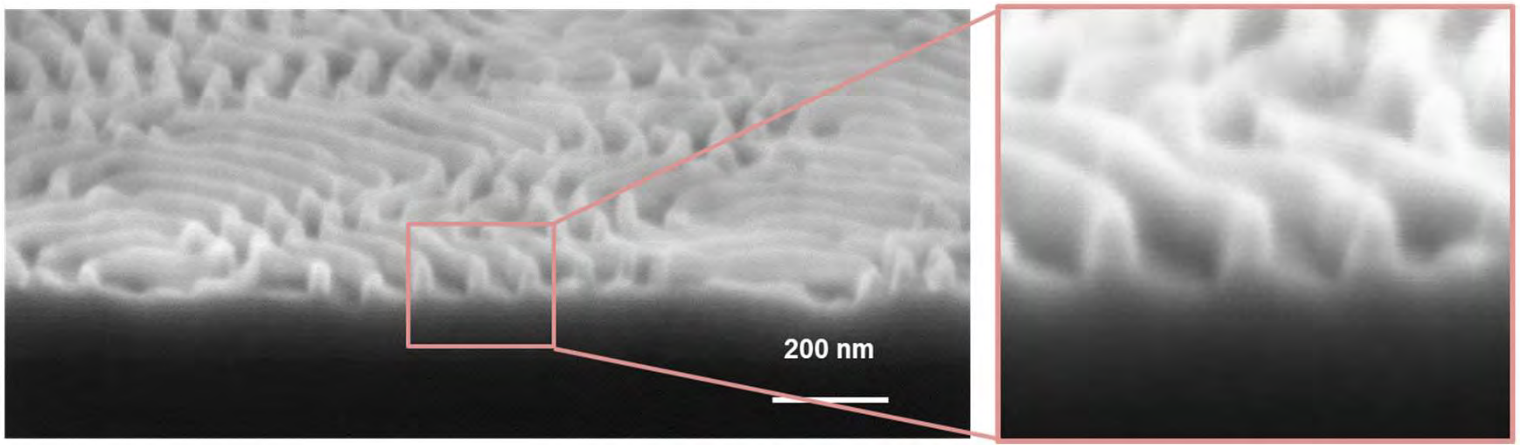


Block copolymer PS-b-PMMA

Pattern transfer

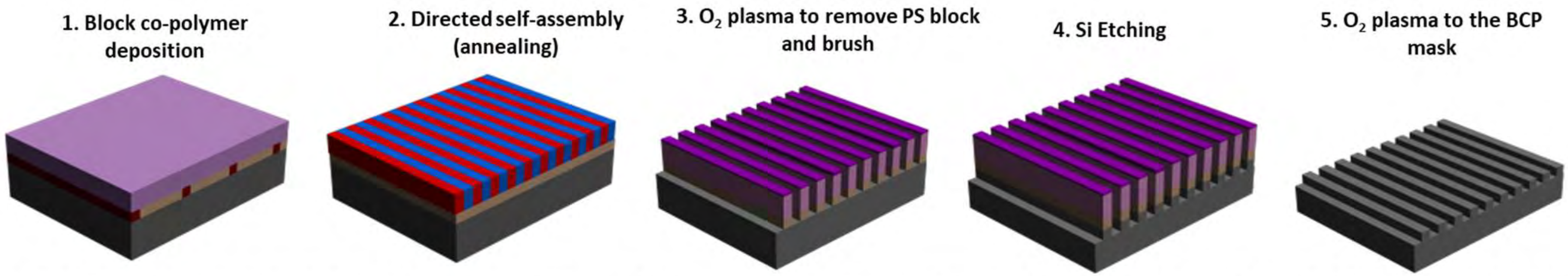
To take full advantage of the nanostructures offered by BCP DSA, highly selective pattern transfer techniques with high fidelity are required

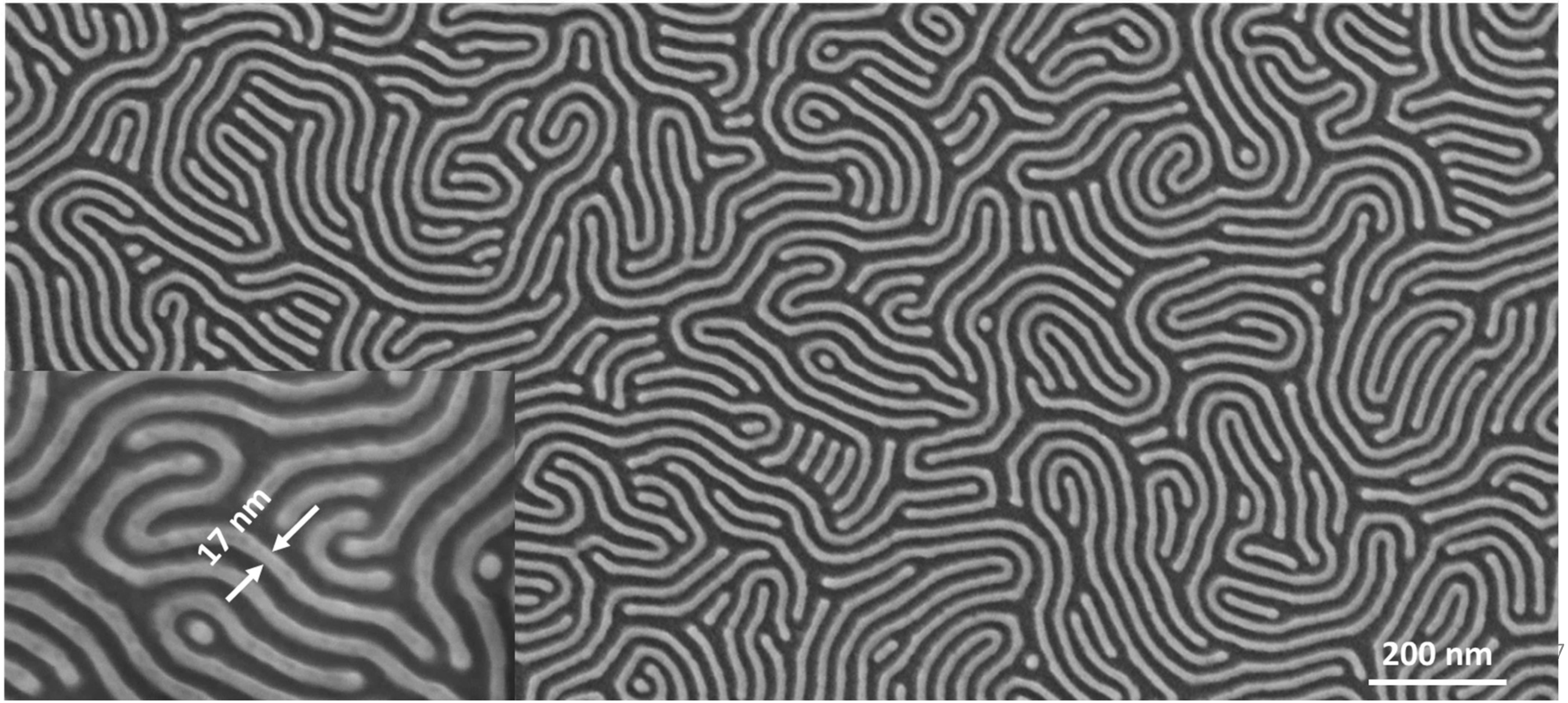




The achievable depth of the etch profile is limited by the thickness of the mask material.

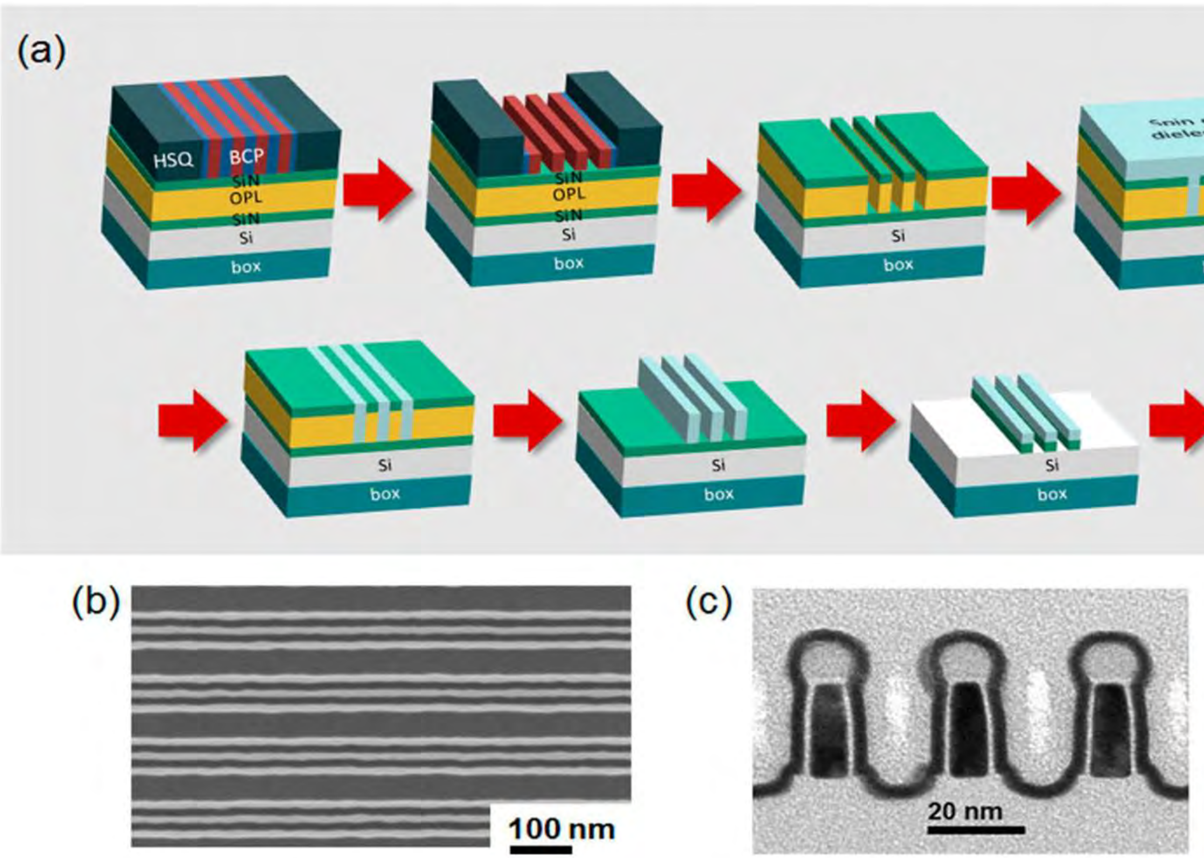
PS-*b*-PMMA 19 **nm hp** transferred to silicon nitride


1. Block co-polymer deposition
2. Directed self-assembly (annealing)
3. O_2 plasma to remove PS block and brush
4. Si Etching
5. O_2 plasma to the BCP mask


17 nm
200 nm

Block copolymer DSA

Two-Dimensional Pattern Formation Using Graphoepitaxy of PS-b-PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication

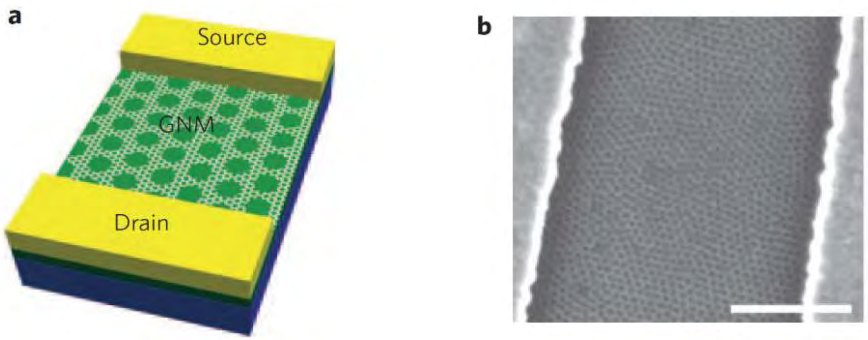


H. Tsai et al. Nanoletters 8, 5227 (2014) (IBM)

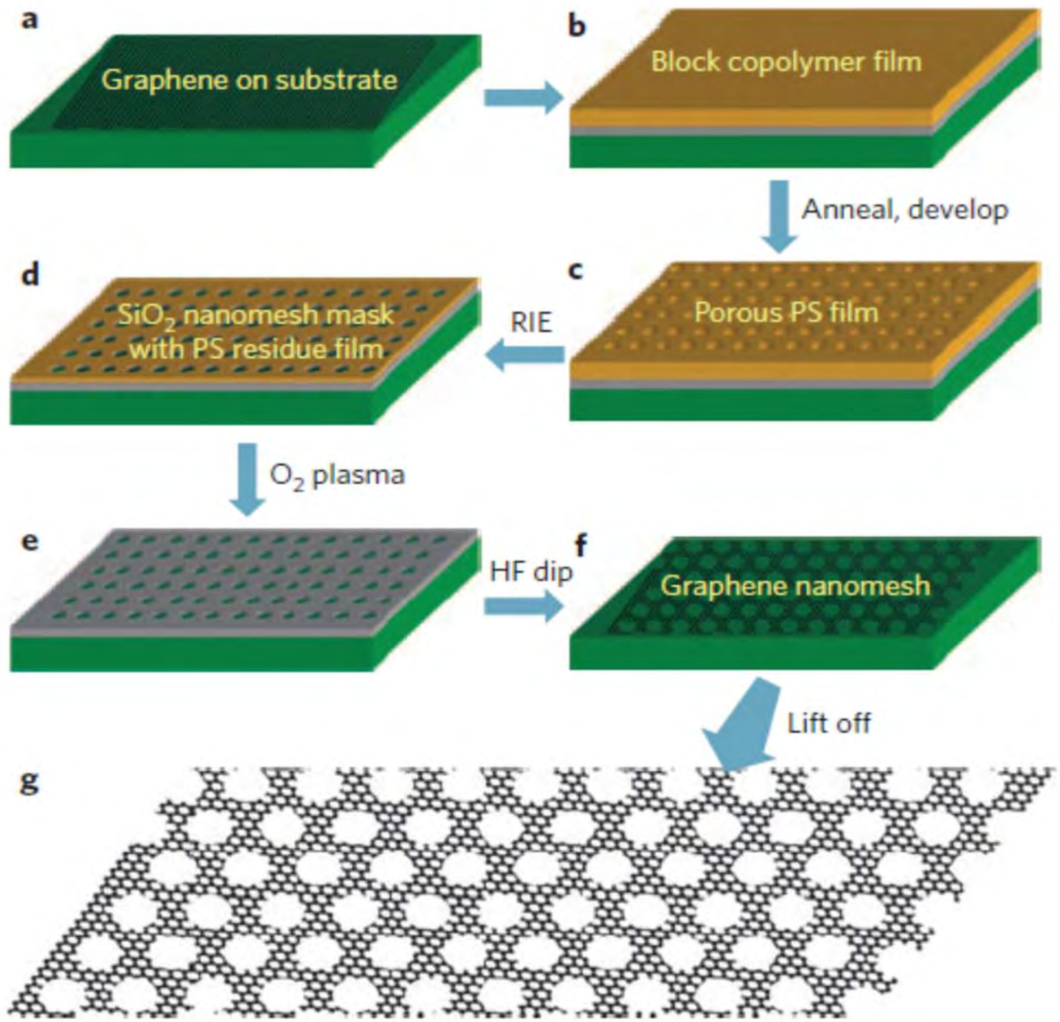
Block copolymer DSA

Graphene has significant potential for application in electronics, but cannot be used for effective field-effect transistors operating at room temperature because it is a semi-metal with a zero bandgap.

Processing graphene sheets into nanoribbons with widths of less than 10 nm can open up a

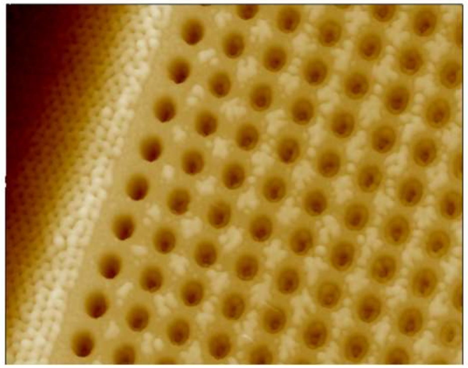


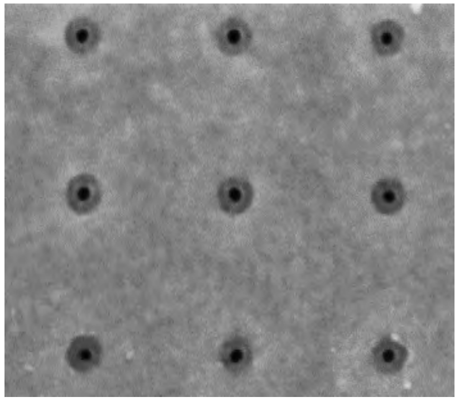
J. Bai et al. Nature Nanotechnology 5, 190 (2010)



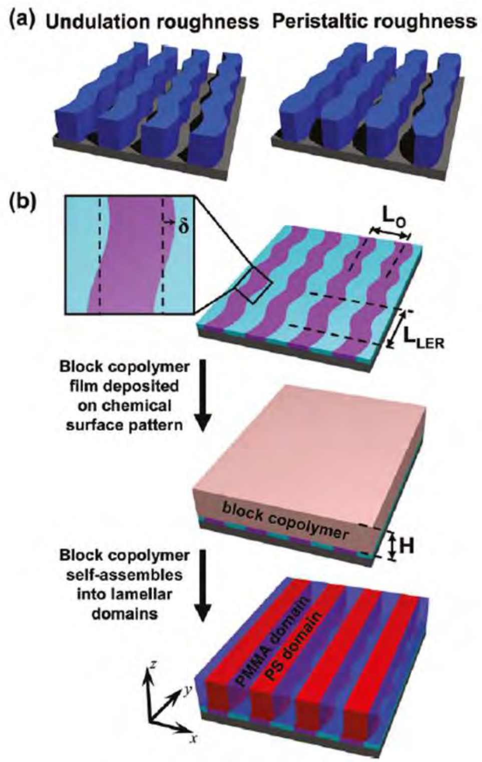
Lithography limitations and bottom-up solutions

- Small contacts and overlay alignment

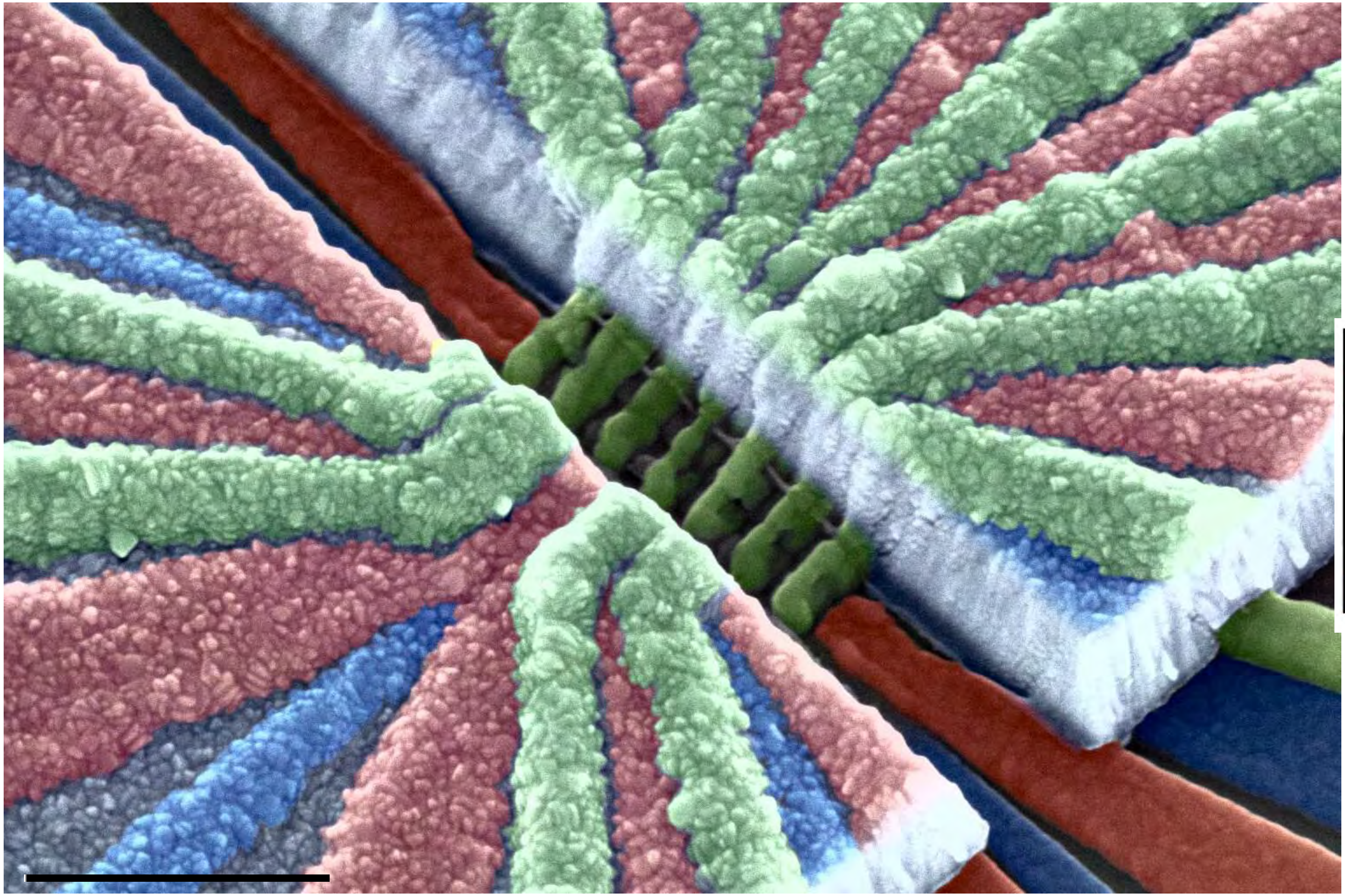




- Line edge roughness

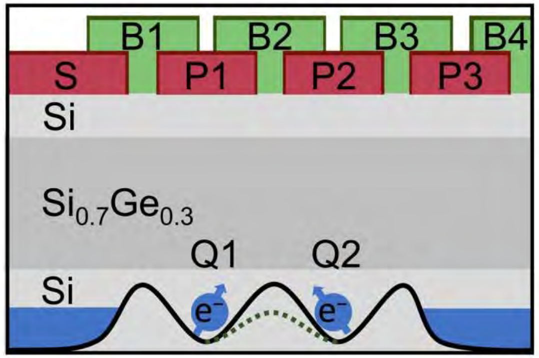


Small contacts needed for semiconductor qubits



Credit: Adam Mills, Princeton University

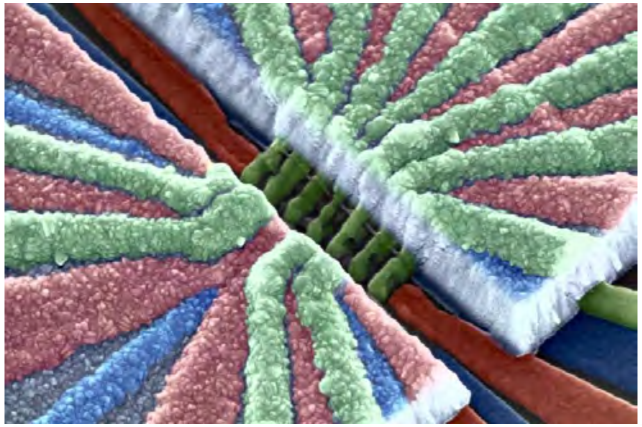
Adam R. Mills et al, Two-qubit silicon quantum processor with operation fidelity exceeding 99%, *Science Advances* (2022).
[DOI: 10.1126/sciadv.abn5130](https://doi.org/10.1126/sciadv.abn5130)

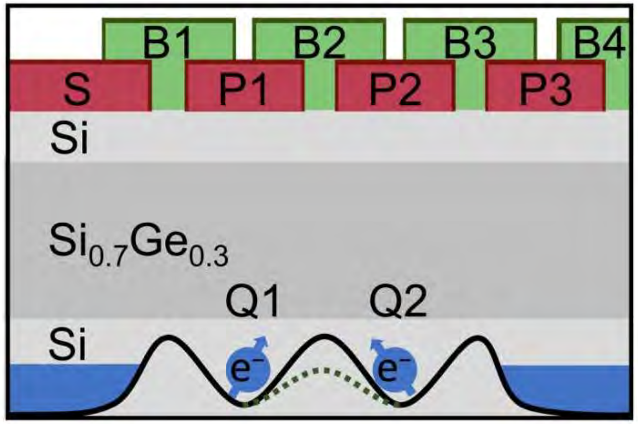


Full two-qubit control in a silicon quantum device, with simultaneous single-qubit control fidelities exceeding 99% and a primitive two-qubit CZ gate fidelity exceeding 99.8%.

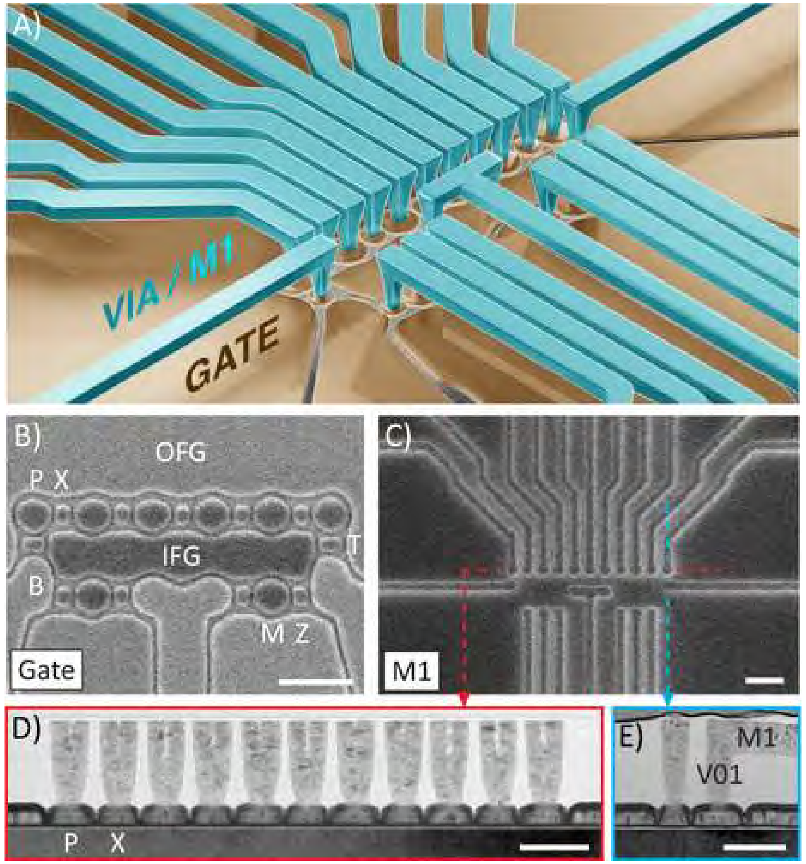
Scale bar: 500 nm

Small contacts areneeded for semiconductor qubits





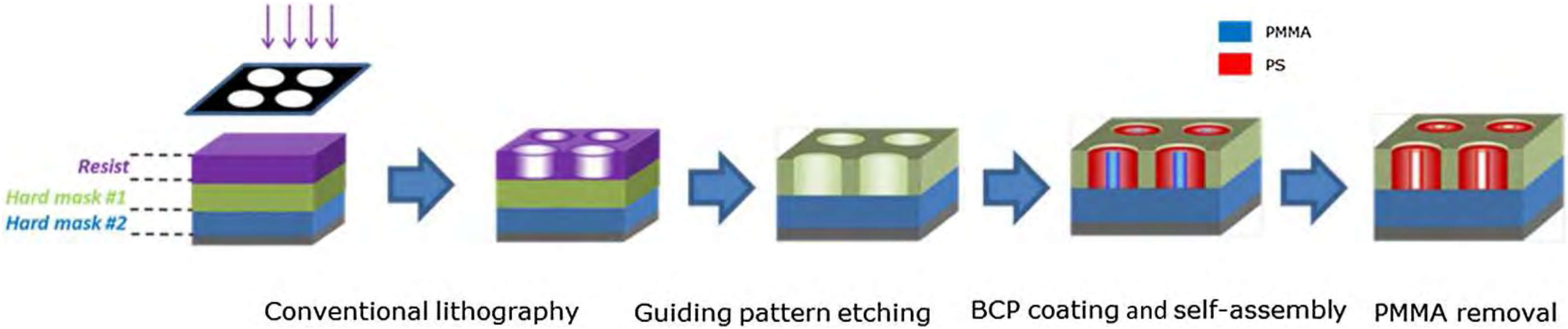
quantum processor with operation fidelity exceeding 99%, *Science Advances* (2022). [DOI: 10.1126/sciadv.abn5130](https://doi.org/10.1126/sciadv.abn5130)

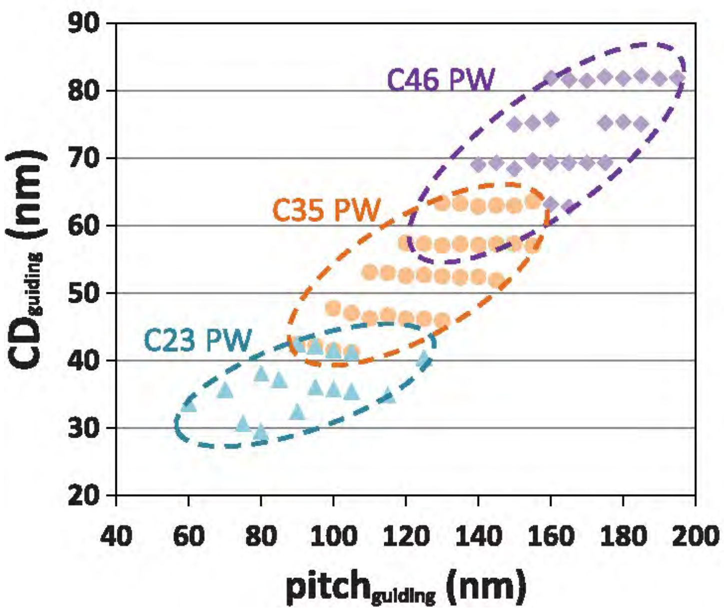


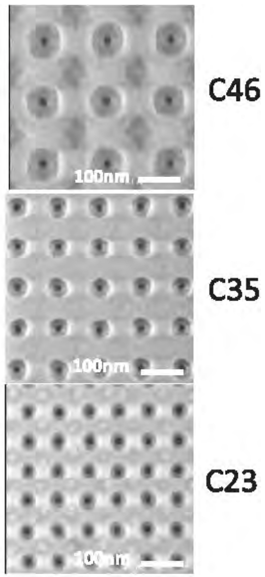
Scale bar:100 nm

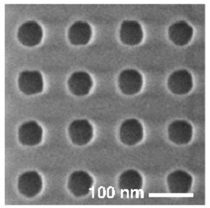
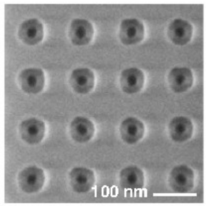
Wonill Ha et al Nano Lett. 2022, 22, 3, 1443–1448

Small contacts by DSA hole shrink



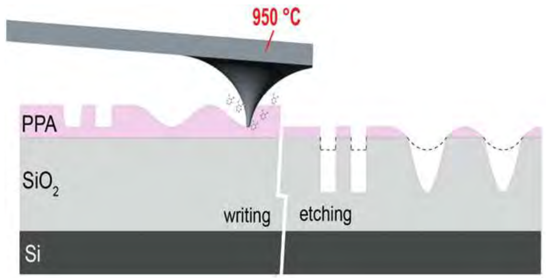


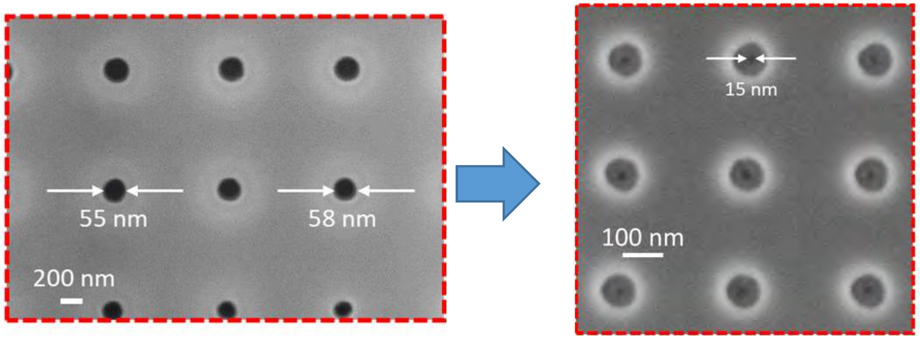


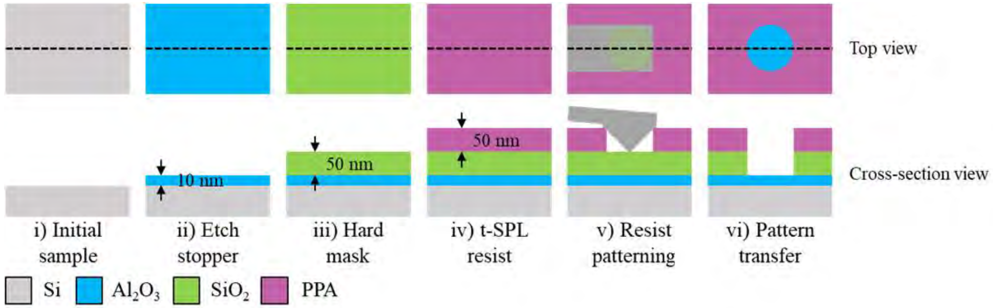
	Guiding pattern	DSA pattern
Mean CD (nm)	54.6	20.3
CDU wafer (nm)	2.8	0.7
SEM image		

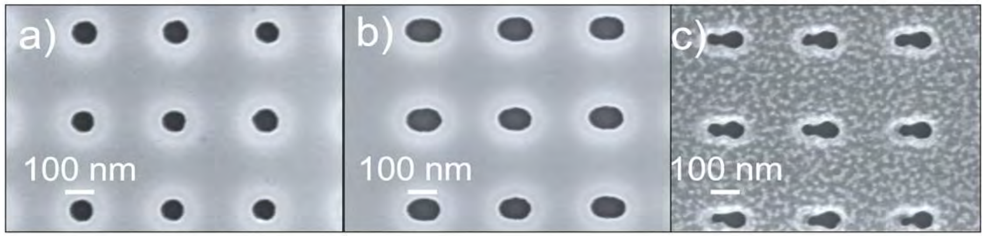
Gharbi, A., Tiron, R., Argoud, M., Chevalier, X., Barros, P. P., Nicolet, C., & Navarro, C. (2015). Contact holes patterning by directed self-assembly of block copolymers: process window study. *Journal of Micro/Nanolithography, MEMS, and MOEMS*, *14*(2), 023508-023508

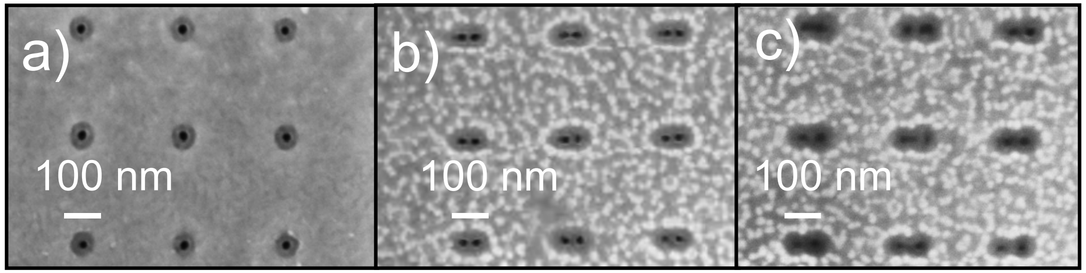
t-SPL and DSA for contact shrink with pattern placement accuracy

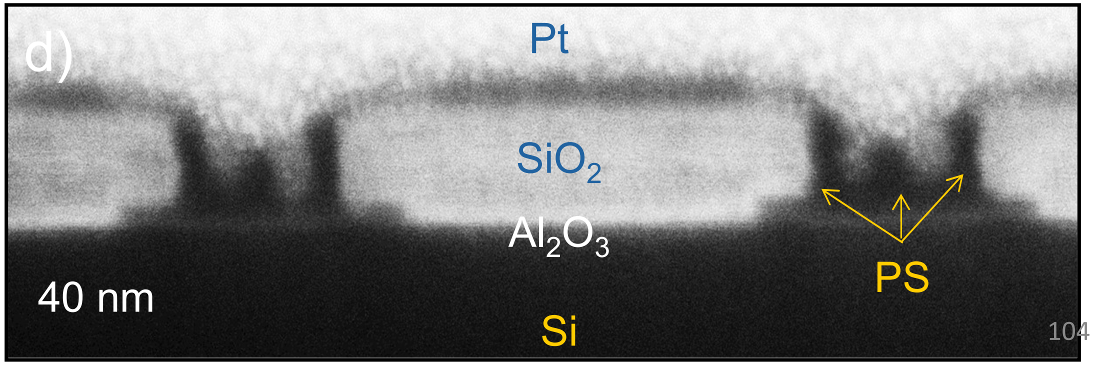






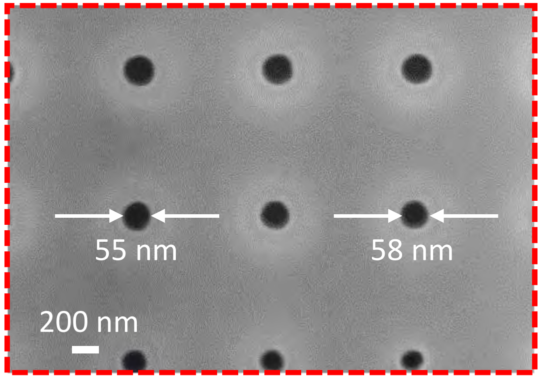


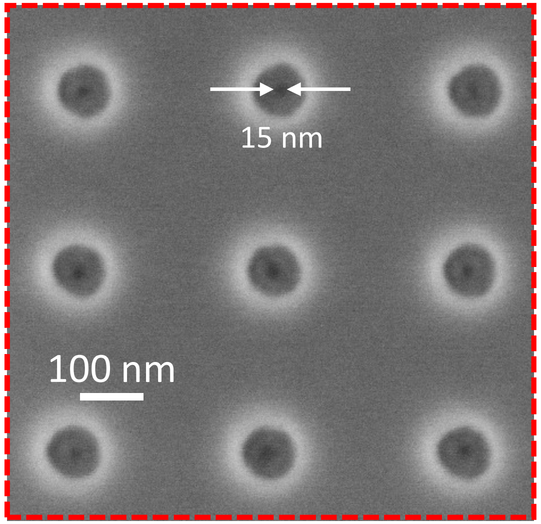


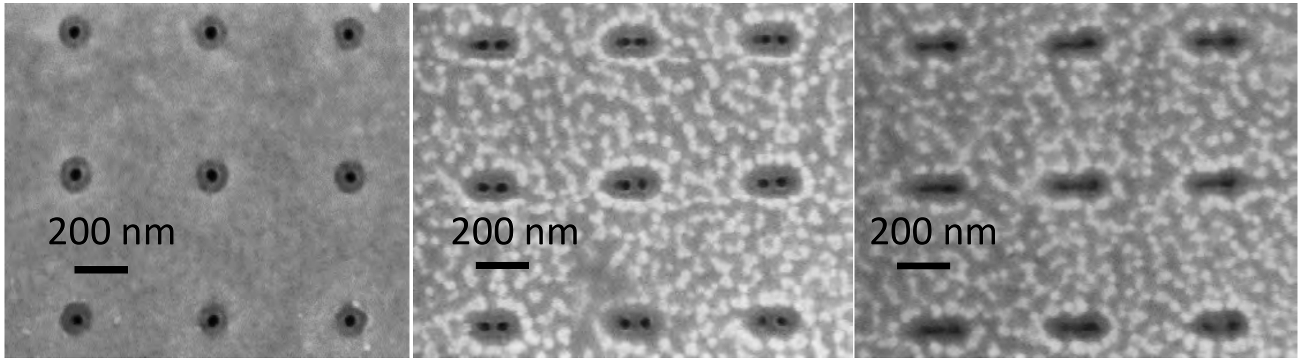


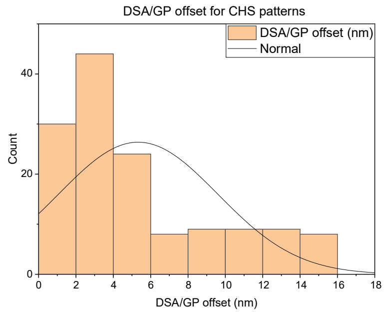
I. Uranga, E. Berke, et al. SPIE Advanced Lithography 2025

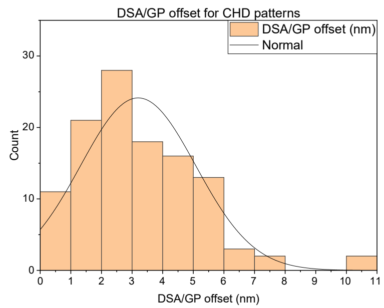
t-SPL and DSA for contact shrink with pattern placement accuracy

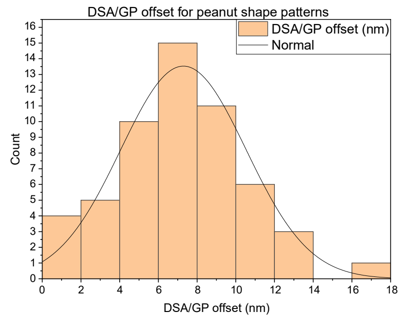












t-SPL and DSA for contact shrink with pattern placement accuracy

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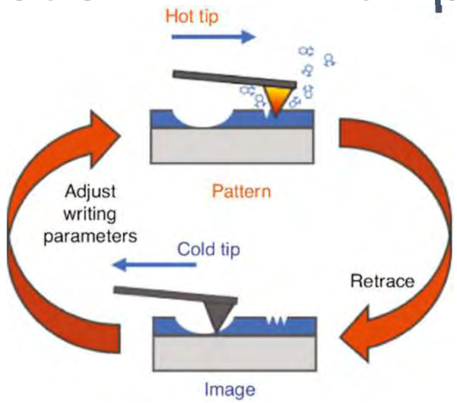
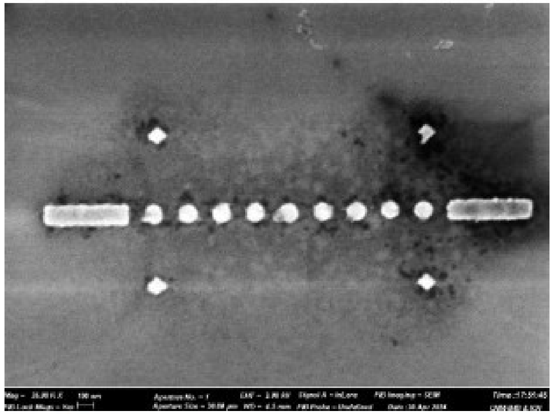
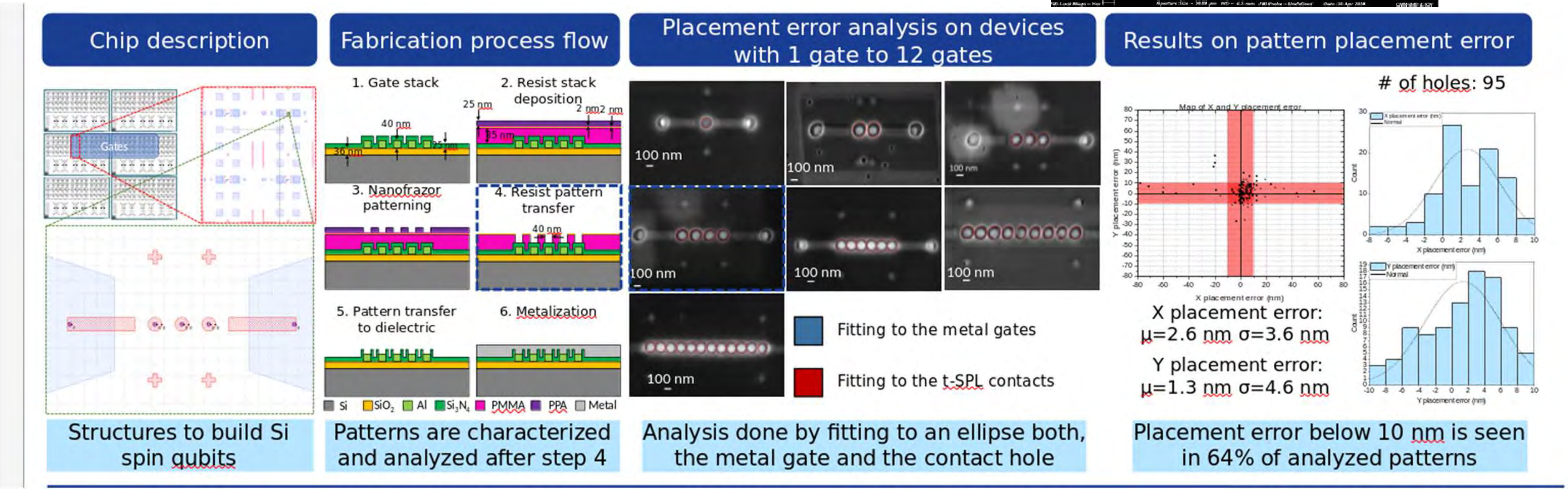


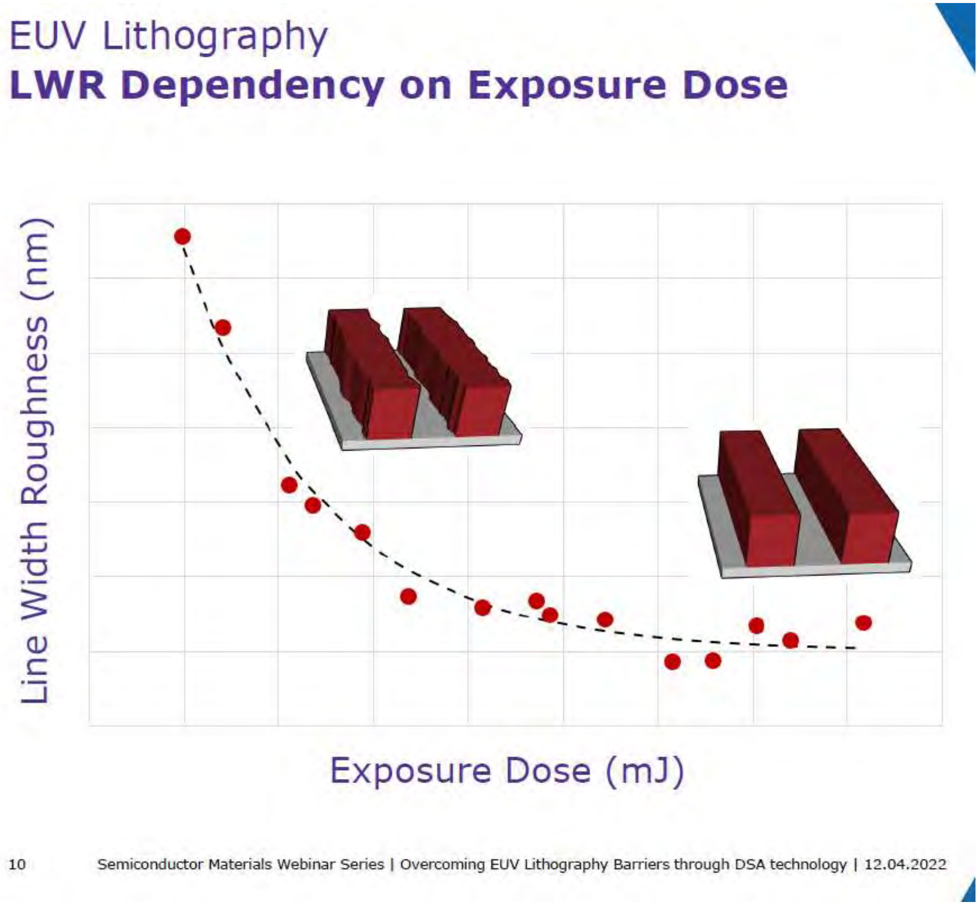


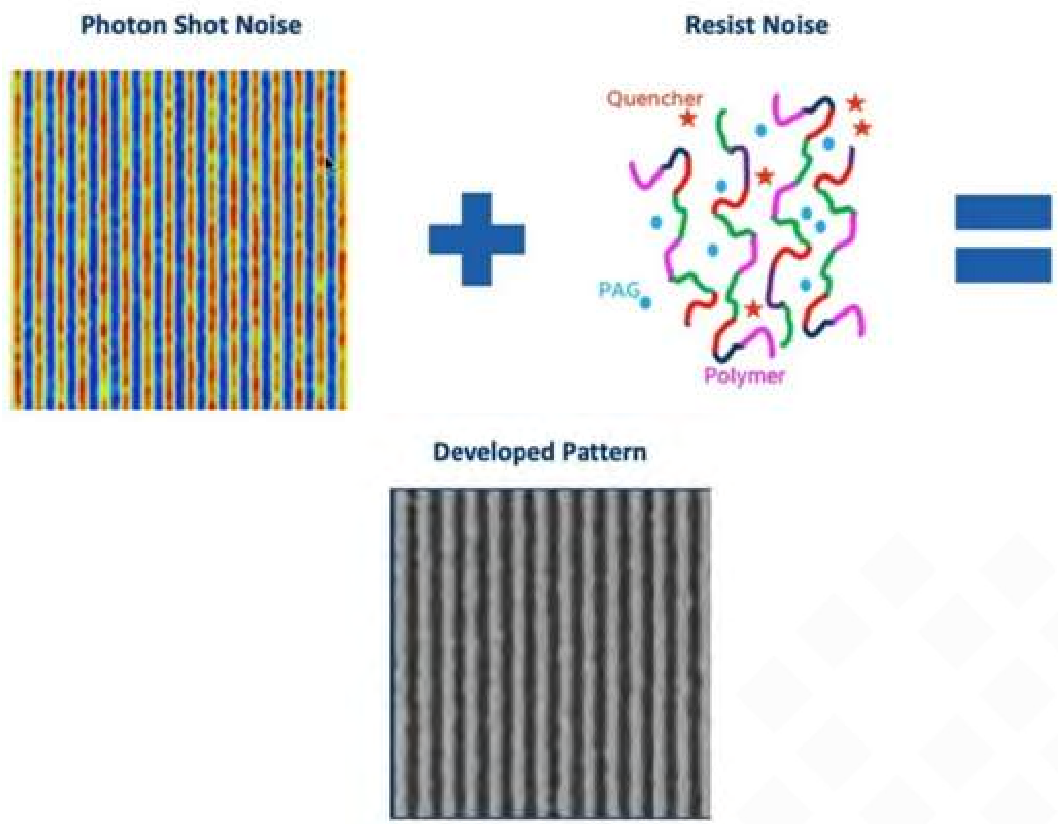


The problem of line edge roughness

- Line Edge Roughness (LER) is the roughness or deviation in the position of an edge as a function of distance along the edge
- It is a significant, stochastic component of CD variability.
- Currently, chemically amplified (CA) resists are used almost exclusively in IC manufacturing in order to maximize throughput. Exposing a CA resist releases acid molecules with a number density that depends on the image intensity, hence transferring the mask pattern information to the wafer.
- . However, the combination of the statistics governing where the acids are released, which is purely a quantum-mechanical phenomenon, with the diffusion of the acid molecules during PEB and the number of acid molecules required to successfully deprotect the resist leads to an issue known as the Resolution-LER-Sensitivity or RLS tradeoff.
- A simple analysis leads to the conclusion that it is inherently impossible to have simultaneously a high sensitivity resist requiring fewer photons per exposure, a low LER and good resolution

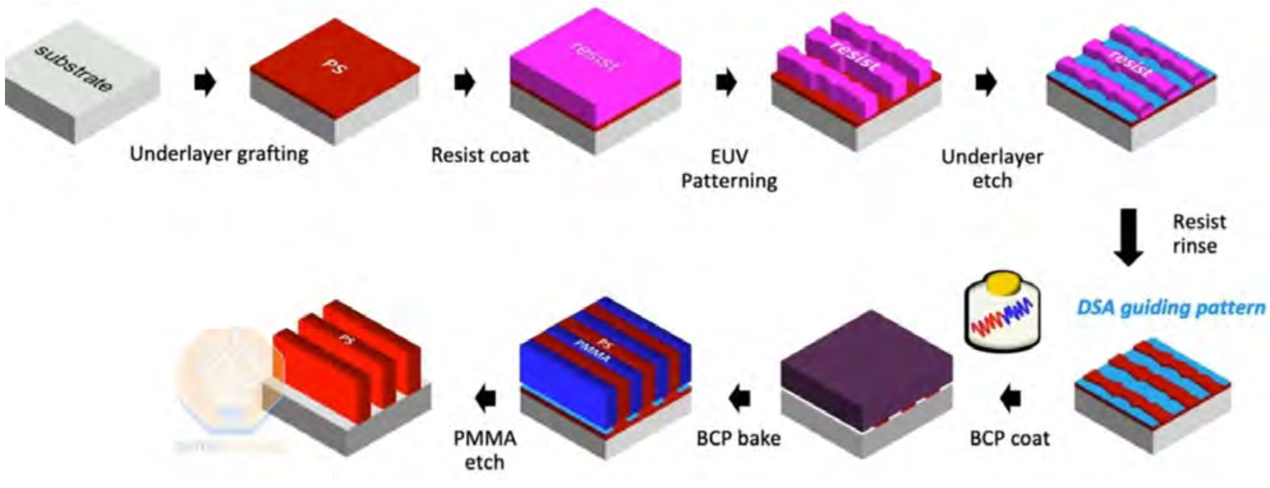
One limitation of EUV lithography (*): line edge roughness





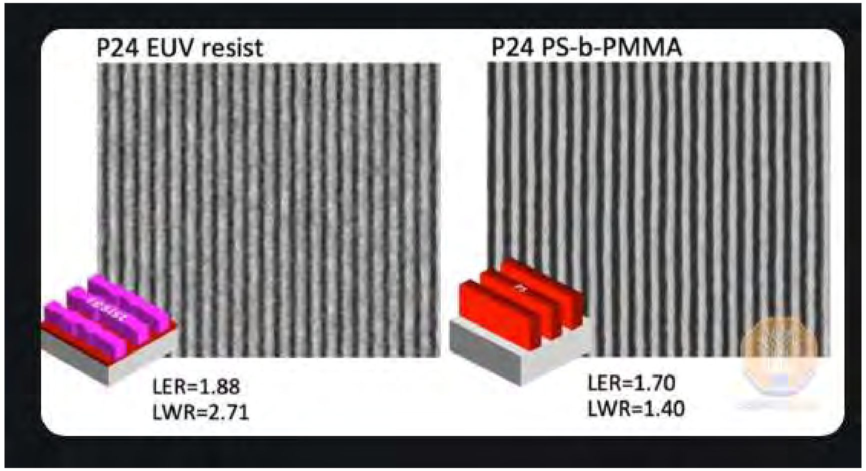
Han, E. et al. "DSA materials and processes development for ≤ P24 EUV resist L/S pattern rectification," Proc. SPIE 12956 (2024)

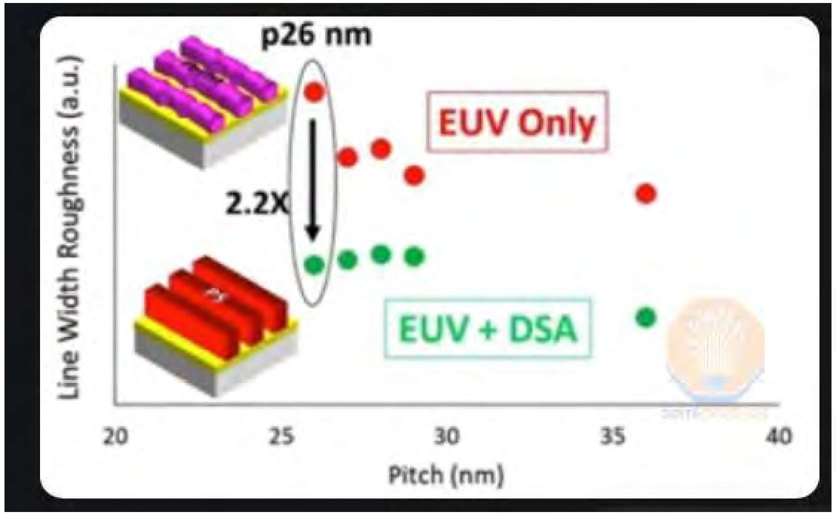
Line edge roughness improvement by DSA



Han, E. et al. "DSA materials and processes development for ≤ P24 EUV resist L/S pattern rectification," Proc. SPIE 12956 (2024)

https://semianalysis.com/





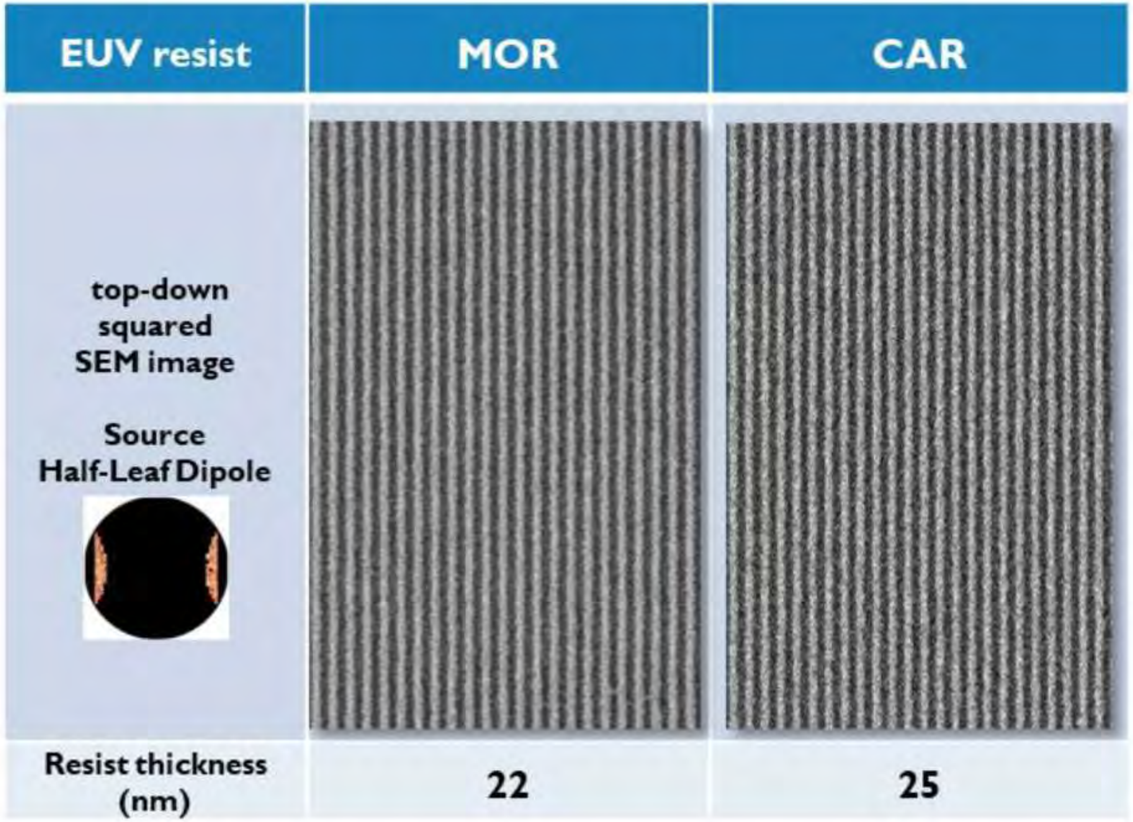


Figure 11. 24nm pitch lines and spaces in MOR and CAR resist resolved with aggressive 0.33NA source.

Metal-Oxide Resists (MOR) are shown to be a good candidate to take over from the chemically amplified resists (CAR) for metal lines.

They are typically thinner and offer a large etch resistance.

Kurt Ronse. Continued dimensional scaling through Projection Lithography. Accepted in Micro and Nano Engineering. 2024.

Beyond processing, the problem of metrology

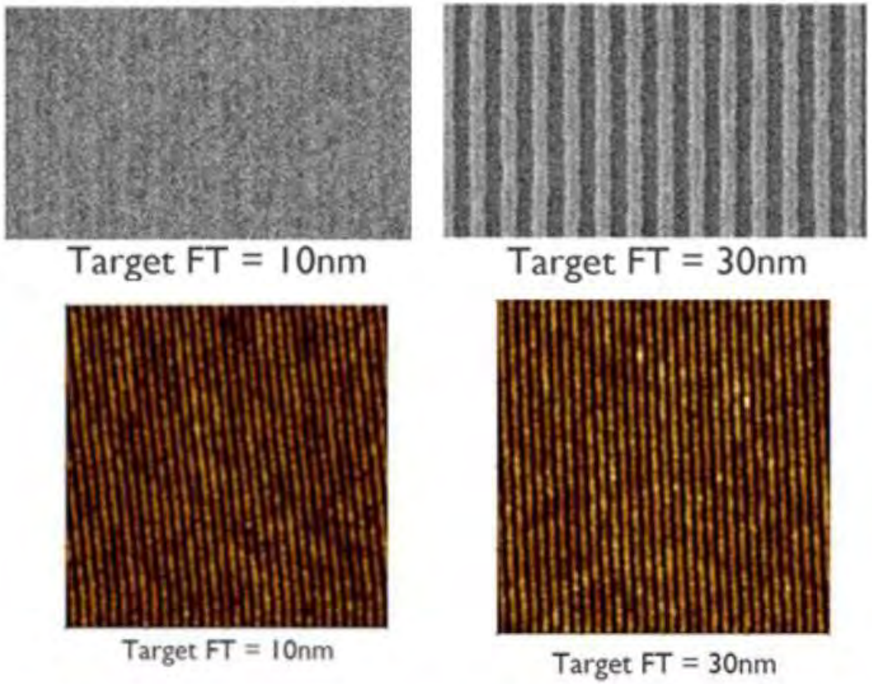


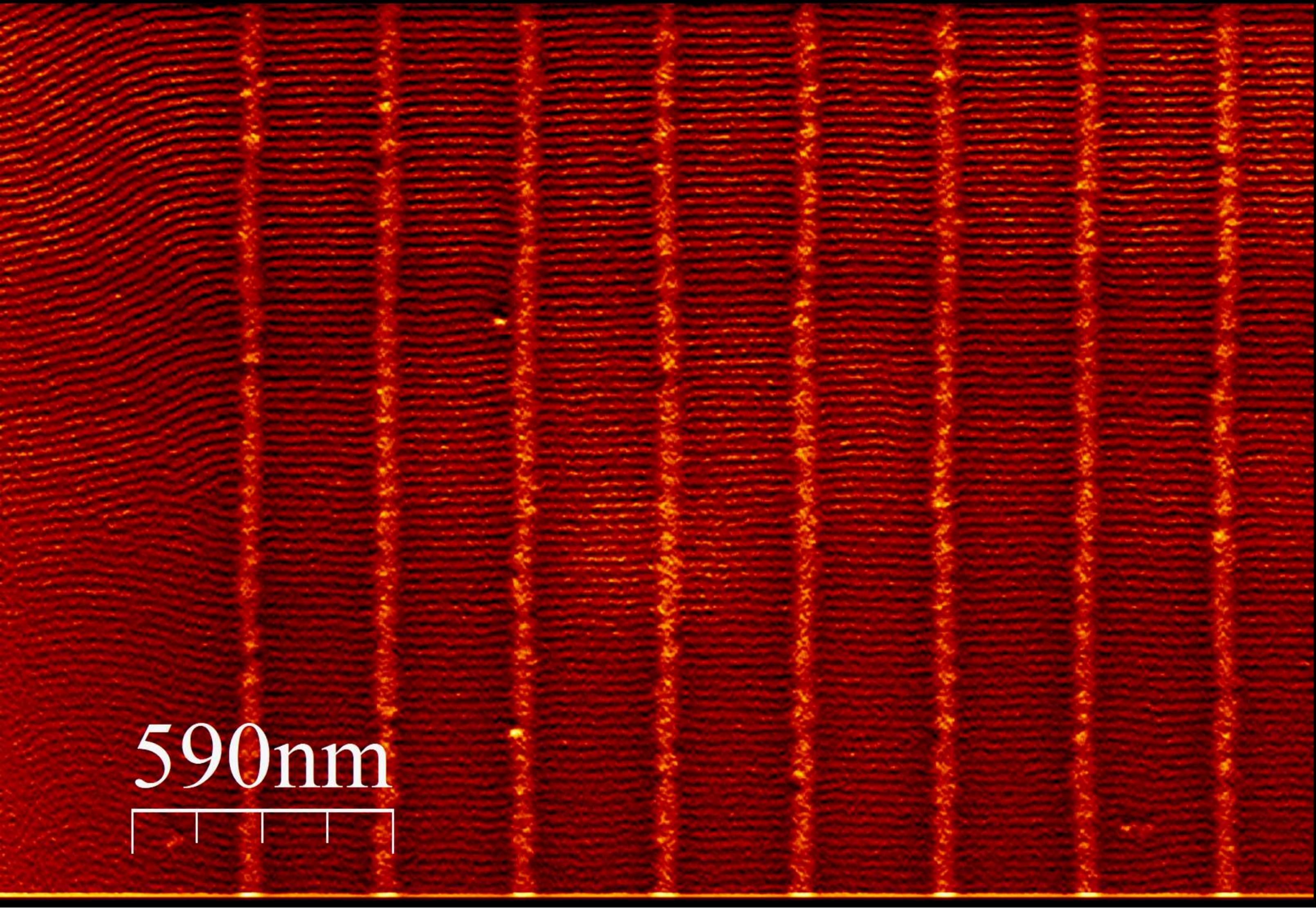
Figure 12. SEM image contrast loss by thinning the film (bottom images are taken by AFM proving that the lines do really exist)

Optical contrast of images of thin films is degrading significantly for CD, roughness, overlay and defect inspection.

Denoising by machine learning [25] is heavily investigated to facilitate metrology.

"Trends in e-beam metrology and inspection", Gian Francesco Lorusso, Proceedings SPIE Volume 12955, 1295515 (2024) https://doi.org/10.1117/12.3010120

Kurt Ronse. Continued dimensional scaling through Projection Lithography. Accepted in Micro and Nano Engineering. 2024.



Patterns form by directed self assembly of block copolymers

Linewidth: 11 nm